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TECHNICAL BULLETIN

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TECHNICAL BULLETIN

Volume Number: 1

Week Number: 45

1.45.1 Subject: "E1 front panel status on C2XX Widebody

We recently encountered a problem on a C2XX Widebody in the field where it would stay up for 20 seconds, then shutdown the PDU's, display a status of "02", then "E1". The problem would recur even after the fan was replaced. The "E1" was an incorrect status. What had happened is that the temperature sensor for the left cabinet power supply fan had failed which in turn, burned a trace on the Front Panel board, giving the false status.
The trace is located on the upper portion of the component side of the board. When the board is installed, the component side is not visible for it is up against the Front Panel. You will need to remove the Front Panel board and inspect the component side. If the trace is burnt off, replace the Front Panel board and the left cabinet power supply fan temperature sensor.
The temperature sensor is located on the top of the metal air plenum for power supply fan which is located on the left side of the PDU.
If you have a Widebody that displays an "E1" status, approach it as fan failure first and if it cannot be resolved in the usual manner, then inspect the Front Panel board for the burnt trace.
This problem has occurred on the floor several times and engineering is looking into it.
Good luck, Chris Magargee

1.45.2 NEC disk drives - Missing part

I'm sending this mail in regard to recent upgrade installation problems. Some of your field expansion cabinets may have an empty NEC disk drive tray slot which has no bracket/screw assembly installed in the back of it. They should have been installed before shipment since they are structured with the trays. Any upgrades of single drives (without trays) will not include this screw assembly. If you are one of the lucky ones without the hold down screw assembly installed in your empty tray slot, please respond to this message and we will send you one. Please include your mailing address to help save time.
Thanks for your help!
Steve Horsmon - Mfg. Quality Dept.

1.45.3 NEC disk drive - New part numbers

Two new part numbers have been released for the 1/2gb NEC D2352A disk drives. They are: 550-000188-290 0.43gb Multibus formatted disk without cables. 550-000188-291 0.43gb VME formatted disk drive without cables.These numbers will enable you to order a formatted disk drive without the cost of additional cables.
Regards, Dave Muir

1.45.4 New Revision IDC

We have just released rev K of the IDC. This rev is intended to correct a situation that caused frequent "loadccu timeout" errors. These errors seem to occur at random and then require multiple sysresets or a full power down to clear.
The rev K is available now, but should not be used to replace current working IDC's. If you are not experiencing the above problem, then do not replace the current IDC for rev K.
Al Haddix

1.45.5 IDC Problem Update

There are several problems with the IDC that you should be aware of.
1. loadccu timeout errors
These errors have been mitigated with the rev K. However, the final fix will be a change to the hardware in the area of the processor chip. Noise is suspected as the cause of problems in the 88K processor phase lock loop circuit.
2. idcfmt
The IDC disk formatter cannot read the manufacturers defect list from the disk. If it is necessary to format a disk, the defect list must be manually entered using the hard copy of the defect list.
Regards, Dave Muir

1.45.6 Slipping Sectors on IPI Disk Drives

The potential for data loss exists when slipping a sector on an IPI disk drive. If a sector to be slipped contains a hard ECC error, and an attempt is made to slip the sector, all data on the track after the sector containing the hard ECC error will be lost.
It is important that you and your customers watch the system error log for recurring ECC errors on the IPI disk drives. A sector that has recurring ECC errors should be slipped before they become hard ECC errors.
With current versions of the IDCU microcode, slipping a sector with a hard ECC error will result in the loss of all data on the cylinder following the sector that is slipped. A sector should be slipped as soon as possible after the second occurrence of a recoverable ECC error. Before slipping a sector that has a hard ECC error, make sure the customer has a current back up of the affected file system since data loss will occur in the bad sector and the balance of the cylinder the sector is located in.
There is no problem when slipping a sector that is exhibiting soft ECC errors.
A solution for this problem has been developed and will be available in the near future.
Regards, Dave Muir

1.45.7 EXP-105 Fan Fail Sense Jumper Plug

During any trouble-shooting of an EXP-105 cabinet fan failure, you may need to bypass a sensor input. To do this will require a jumper plug.
There is no part number for the jumper as an assembly. The part numbers for the individual parts can be ordered and assembled locally.
The part numbers are:
304-000004-002 Four position connector shell
314-001010-001 20-14 awg socket.
Obtain the wire from a local source. Sorry for the "kit" approach, but the jumper plug is not stocked in manufacturing.
Kelvyn Gipp

1.46.1 EXP-105 Power Controller

Last week's bulletin contained part numbers for parts to build an EXP- 105 Power Controller sensor shorting plug.
The assembled shorting plug is now available using one part number:
Part No. 603-010030-200
Kelvyn Gipp

1.46.2 3480 Tape sub-system Installation Prerequisites

System prerequisites to installing this product are as follows:
8.1 ConvexOS 3.5 DDB (Diagnostic Data Base) 3.4 System Diagnostics Rev J VIOP
Kelvyn Gipp

1.46.3 C210 to C220 Upgrades

We have, in the past, had some difficulties when adding a head to a C2 10. These problems encountered have been anything from a defective board in the new head to a bad net on the head A side of the backplane.
In order to counter these possible problems, I would like to recommend that when attempting this upgrade that the boards in the old head (head B) be moved to the head A slots. This would then allow the new boards to be installed in the previously used slots in head B.
If you should encounter a problem after the upgrade, then this will allow you to know immediately if you are experiencing a backplane problem with the slots in head A or the new boards installed in head B.
This procedure will eliminate a lot of guess work and help you restore the customer to operation in the quickest manner.
Al,

1.46.4 VIOP to VBCU Cable Removal

It is important that all FE's understand that cables between the VIOP and the VBCU should never be removed with power applied to either the VME chassis or the VIOP.
This action can result in damage to the cable driver on the VIOP and render the CCU inoperative.
Al,

1.46.5 Adding a Third VME Tape Controller

Should you ever need to add a third (or more) VME Tape controllers to a system, then you will need to insert an additional entry in the /usr/sys/sysgen/REL_C2 file, as follows:

REL_C2 before
controller type MTC-201 at csr 0x000 int 1
unit 0 type MTD-201
unit 1 type MTD-201
controller type MTC-201 at csr 0x000 int 1
unit 0 type MTD-201
unit 1 type MTD-201

REL_C2 after addition:
controller type MTC-201 at csr 0x000 int 1
unit 0 type MTD-201
unit 1 type MTD-201
controller type MTC-201 at csr 0x000 int 1
unit 0 type MTD-201
unit 1 type MTD-201
controller type MTC-201 at csr 0x000 int 1
unit 0 type MTD-201
unit 1 type MTD-201

Please note; the controllers are the key part of the entry. The "unit" entries are for reference only, and it is not necessary to have four "unit" entries for each controller. The "after" configuration will allow the system to access up to 12 tape drives on the three controllers.
It will be necessary to do a sysgen and reboot the system after making the changes to the REL_C2 file.
Our thanks to Phil Kemp for providing this information.
Kelvyn Gipp

1.46.6 "E1" Front Panel Status Update

This is a correction to the Technical Bulletin, Vol. 1, Week 45. The probe in the air plenum on the power supply fan is an air flow sensor, not a temperature sensor.
It has a part number of 410-000193-200. I hope this did not cause any confusion.
Chris Magargee

1.46.7 Tech Tip Updates

The October issue of Tech Tip updates and Revision History documents is in the mail. For those receiving Tech Tips, please IGNORE the instruction on the COVER SHEET to ADD CPU-027 and CPU-028. This instruction was overlooked prior to the COVER SHEET being printed.
The Revision History documents are correct as printed.
Thanks
Dan Schoner

1.46.8 C1 Diags. 6.6 Install Problem

Recently we have had several occurrences of the install script for C1 V6.6 diags failing. The failure message says "no cop_out found" (actually looking for cop.out). If this should happen you should first try a ".diaginit -f". If ".diaginit -f" is not on the spu disk you will need to load C1 System Diags. Version 6.5, do the ".diaginit -f" and then load C1 System Diags. Version 6.6.
Also remember that ConvexOS Version 9.0 on a C1 systems requires the following:
SpuUnix Ver. 5.2 Diag Data Base Ver. 2.7 System Diags. Ver. 6.6
Regards,
Dan Brenner

1.46.9 Disk Information Needed

In order to accurately track NEC 1.1gb reliability (and have HDA's replaced under warranty) we need to get information on the failures at secure sites.
If you support secure sites that have had disk failures that required replacing the disk drive and the entire drive was left on the account, please send the following information: Serial number of the drive or HDA, month and year of the failure, and if possible the date the drive was installed. Please email the information to Brad Jones - bjones.
Regards
Dave Muir

1.47.1 NEC Disk Drive Replacement

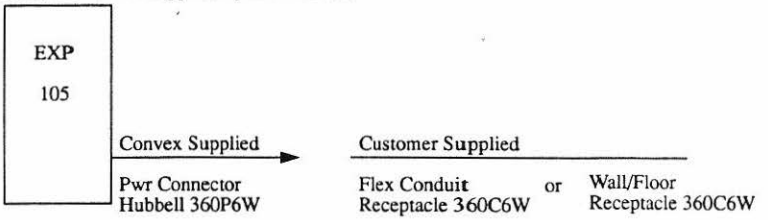
When a NEC disk drive is replaced at a secure site, please attempt to arrange the return of the disk chassis minus the disk platters. If it is acceptable to the customer, the disk platters can be removed from the HDA, and the HDA housing left in the chassis to facilitate mounting the logic boards. A new HDA can be installed in the chassis which will save considerable money for Convex.
Regards,
Dave Muir

1.47.2 PIA 603 Errors on C220's

We have recently encountered some new errors on recent C220's. By new, I mean those with serial numbers above 8500.
These new problems manifest themselves as PIA 603 errors. This error seems to be the result of new components being used on the board that required different tuning.
So, if you encounter a PIA 603 error, please replace the CPX and return the defective one. The rev of the CPX must be L in order to correct this problem. Any rev lower will not solve this problem.
Al,

1.47.3 EXP-105 AC Power Connectors

The following diagram describes the power connectors that are supplied with the EXP-105 and the connectors that must be supplied by the customer.



Kelvyn Gipp

1.48.1 New EDC/EFU with RITA/VAL gate array

We have finally shipped our first new EFU/EDC's with the new RITA/VAL gate arrays installed. These boards were shipped to GE Astro for an upgrade. These boards will have a new part number as follows:

EDC 410-002219-200
EFU 410-003220-200

The intention is to upgrade all systems in the field with mostly 240's to be accomplished first. This complete upgrade will take approximately 18 months with the 20 head sets that will be available. The co-requisites for these boards are as follow:

1) 3.7 diagnostic database
2) 3.5 diagnostics
3) 5.2 spu unix

Without this new software the new boards will not function. If 3.7 is not installed the system will not even boot. If 3.5 is not installed then the gate arrays will not function as designed. The diagnostic for these gate arrays is located in misc4000.
New systems shipped after Dec. 31 will include these new gate arrays. Nothing shipped this quarter will contain the new boards.
These new EFU/EDC's will work with the current boards. There will be no compatibility problems between the current modules and the new modules.
These new modules are the solution to the 904/201 crash problem. It will still take a constant effort to take care of current situations until these systems can be upgraded.
Al,

1.48.2 Reporting Slipped IDC Disk Sectors

In an effort to reduce the burn in time for the new Seagate IDC drives, it is requested that all slipped sectors on these drives be reported to Chip Stroup after it is accomplished.
This reporting must be accomplished whether the slipped sector is accomplished by the TAC or in the field. So please, after every slipped sector is accomplished, please send email to stroup@convex.
Thanks.
Al,

. . .continued on next page. . .

1.48.3 Memory Capacity Configuration Chart

The CONVEX Theory of Operation (C200 Series) Document No. 081-005030-000, dated September 1990, page II.5-24, lists the following table:

Table 5-4, MAM to MCM Configuration

MCM	MAM SIZE				
	4 Mbyte	8 Mbyte	16 Mbyte	32 Mbyte*	64 Mbyte*
1 MCM	16 Mbyte	32 Mbyte	64 Mbyte	128 Mbyte	256 Mbyte
1 MCM Pair	32 Mbyte	64 Mbyte	128 Mbyte	256 Mbyte	512 Mbyte
2 MCM Pair	64 Mbyte	128 Mbyte	256 Mbyte	512 Mbyte	1 Gbyte
3 MCM Pair	96 Mbyte	192 Mbyte	384 Mbyte	768 Mbyte	1.5 Gbyte
4 MCM Pair	128 Mbyte	256 Mbyte	512 Mbyte	1 Gbyte	2 Gbyte

* Since this table is referring to MAM configurations (MCM1 's), the last two columns (32 Mbyte and 64 Mbyte) are not valid configurations. The 4th column (32 Mbyte) capacities are currently available in C2 widebody systems with MCM2's (utilizes mimes) but not in the narrow body C210 or C220 systems.
Next year, MCM3's are scheduled to be released and at that time 2 Gbyte configurations will be possible.
Jerry

1.49.1 Updated and New FMI's

The following FMI's were released this week. You should be receiving copies of them within the next 2 weeks.

FM0067-B. Added new step 28 on page 5. This addresses the "SYS ID" jumper that tells the SCM if the system is a C201/202 or C210/220.

FM0081. (C2xxW's) Reduce crosstalk from FUDASDFSQ to SPBPDMODE. This crosstalk induced failures with a variety of symptoms including false errors in "dcache" dumps and true #904 rita ram parity errors while running OS. These symptoms are exhibited particularly with EFU's serial number 710690 and above. If the backplane being upgraded is a rev.B,C,D or E, it will not be a true rev.G when this FMI is completed and you SHOULD NOT mark the backplane rev. G on the revision level tag. If the backplane being upgraded is a rev.F, it will be a true rev.G when this FMI is completed and you SHOULD mark the backplane rev. G on the revision level tag.

FM0082. (C2xx's) Reduce crosstalk from FUAASAFSQ to SPBPADMODE. This crosstalk induced failures with a variety of symptoms including false errors in "dcache" dumps and true #904 rita ram parity errors while running OS. These symptoms are exhibited particularly with EFU's serial number 710690 and above.

FM0083. Upgrade to new RITA and VAL gate arrays to resolve the random 201 and 904 errors. System must have FM0081 for C2xxW's and FM0082 for C2xx's. System must have Spu Unix 5.2, Diag. Data Base 3.7 and System Diags. 3.5

Dan Brenner TAC/HW

1.50.1 New EFU/EDC vs PM

With the release of the new gate arrays for the EDC/EFU's periodic pm's have become imperative. With these new gate arrays, it is possible for the RITA circuitry to be broken with no visible indications. Because of this potential it is necessary to run the following diagnostics on a reasonably frequent basis:
1) misc4000
2) cpu4233 -s 500-575
3) cpu4231 -s 500-519
These diagnostics will insure the proper performance of this new hardware.
Al,

1.50.2 KNOWN C2XX PROBLEMS

1. FLOW WRONG ANSWERS OCCUR IN RP INTERMITTENTLY. (EDC/EFU ONLY)

2. DEV 5130 -C 1, WHEN 2 DRIVES ARE CHAINED ON A CONTROLLER IT WILL NOT READ THE FLAW DATA CORRECTLY FROM THE DISK. B. JONES

3. 16 WAY INTERLEAVE WILL NOT MMINIT WHEN 4 PAIRS OF MCM'S WITH DIFFERENT SIZE MAM'S ARE INSTALLED ON SOME PAIRS. LOWDERMAN [12993]

4. SPURIOUS INTERRUPTS FROM THE 68000 ON THE MIOP WILL OCCUR IF A MARGIN COMMAND GOES OUT DURING A PROCESS. D. MALONEY [12998]

5. SYSRESET CPUS -1 2 IS NOT A SUBSET OF SYSRESET -1 2. REED [12991]

6. IDC DIAGNOSTICS ARE NOT ACCEPTABLE TO DIAGNOSE DISK PROBLEMS ON IPI DISK DRIVES. STROUP FEB. '91

7. COPMOD DOES NOT WORK ON THE C230I MACHINES. HARRIS

8. INSTALL SCRIPTS RUNNING ON A C230I STOP WHEN TRYING TO START MEM4000. THE FAILURE MESSAGE IS: NO CPUS REFLECTED IN DIAG_DB: TERMINATING, FAILURE IN ANSWER GENERATION, ABORTING SCRIPT GENERATION, SW ERROR: UNABLE TO OPEN LOG. HARRIS/DOUTHITT

9. WITH THE -122 EPROM ON THE 168 SCM A BAD PS6 WITH NO DC OUTPUT HANGS THE SCM INSTEAD OF SHUTTING THE SYSTEM DOWN. PHELAN

1.50.2 KNOWN C2XX PROBLEMS (continued)

10. ENVIRONMENTAL ERRORS CAUSE IMMEDIATE POWER DOWN OF THE SYSTEM. COULD A TIME DELAY BE IMPLEMENTED SO THAT AN ORDERLY SHUTDOWN BE ACCOMPLISHED? ABERNATHY

11. THE DEFAULT TIMEOUT ON CPU4231 NEEDS TO BE LONGER. IF YOU HAVE A C201 THE TEST WILL TIMEOUT ON ONE SUBTEST WHEN YOU RUN DEFAULTS. IF YOU BOOST UP THE TIMEOUT FACTOR IT WILL PASS. REED

12. DUAL PI2'S WILL NOT WORK RELIABLY ON C240'S. RECOMMEND LOADING ONE PBUS BEFORE ADDING A SECOND ON ALL CONFIGURATIONS. STROUP FEB. '91

13. IDC DATA COMPARE PROBLEMS. 2K AND 4K SIZES. STROUP 2K PROBLEM FIXED WITH NEXT uCODE RELEASE, 12/90. 4K PROBLEM TO BE FIXED WITH 9.0 OS.

14. CPX4000 -S 185 WHEN RUN MANUALLY FROM DSHELL WILL GET THE FOLLOWING ERROR MESSAGE: FAILED: INVALID PCM REFERENCE HARD ERROR CLEAR WHEN EXPECTED SET CPX BANK: A EVEN ADDRESS: 0X00000000 A SYSRESET CPUS -1 2 WILL FIX THE FAILURE. REED (CONTACT FILED)

15. MMINIT, IF YOU HAVE BOARDS INSTALLED IN PAIR 0 AND 2 WILL GIVE YOU THE FOLLOWING MESSAGE: MEMORY PAIRS 0 AND 2 MUST BE INSTALLED FIRST FOR MAXIMUM INTERLEAVE USING 8 WAY INTERLEAVE. THE MESSAGE SHOULD READ PAIRS 0 AND 1. REED (CONTACT FILED)

16. IDC format on 4.1 ucode will not reliably format drives when unknown error codes are encountered. Carruthers FIXED IN NEXT UCODE RELEASE

17. Manufacturing flaw maps cannot be read with 4.1 IDC ucode. Carruthers FIXED IN NEXT UCODE RELEASE

18. Cannot reliably slip sectors with 4.1 IDC ucode. Carruthers FIXED IN NEXT UCODE RELEASE.

19. LOCK MANAGER IS BROKEN ON THE IPI DISK DRIVES. CARRUTHERS (CONTACT FILED)

20. FILE PATH IN DB_idc DOES NOT WORK WITH idcfmt IN THE DIAGNOSTIC DATABASE. CARRUTHERS (CONTACT FILED)

1.50.2 KNOWN C2XX PROBLEMS (continued)

21. idcfmt REPORTS LOST SYNC BYTES INCORRECTLY. CARRUTHERS (CONTACT FILED)

22. C1 6.6 DIAGNOSTICS DO NOT LOAD IO4000. REED (CONTACT FILED)

23. CXPA 1.2 HAS PROBLEMS AND CANNOT BE SHIPPED PER GARY BROOKS.

1.50.3 ECO installation

In order to accomplish the recently released FMI's it will be necessary for each FE to obtain the necessary pins and coax from logistics. It is important that all FE's maintain these parts as it is never known when a backplane problem may arise.
For your convenience I include the part numbers for the minimum that should be on hand:

Description	Part Number	Qty.
C2 BACKPLANE REPLACEMENT PINS	314-000121-001	10
C2 BACKPLANE INSULATED PINS	314-000120-001	10
PIN, C-PRESS ISO CONTACT MODIFIED (FLEX)	314-000130-500	10
50-OHM CO-AXIAL	613-000019-001	10'
30 AWG TWISTED PAIR WIRE	613-000020-001	10'
30 AWG WIRE	613-000007-001	10'
B/PLANE PIN REMOVAL/REPLACEMENT TOOL	AMP P/N 265871-1	1
SOLDER, Almit Al,	No P/N Assigned	5'

1.50.4 Diagnostics

Whenever you set the "Forced Faulting Enabled" option "= y (yes)", within a diagnostic program, you **MUST** also increase the value for the "Timeout Scale Factor Enabled" option to between 25-30. Errors may occur if this value is not increased when no problems exist.
Kelvyn Gipp

. . .continued . . .

1.50.5 New IPI disk part numbers

New part numbers for formatted IPI disk drives have been issued. These are replacement drives, and have been formatted prior to shipment. This will save time during the installation of a new or replacement drive on a system.

FRU, IPI Disk Drive, 6mbs - 550-000306-297
FRU, IPI Disk Drive, 3mbs - 550-000303-297

Just a reminder on other disk part numbers.
FRU, VME formatted 1.1gb - 550-000192-291
FRU, VME formatted 0.5gb - 550-000188-291
FRU, Multibus formatted 1.1gb - 550-000192-290
FRU, Multibus formatted 0.5gb - 550-000188-290

Regards,
Dave Muir

1.50.6 HPPC Power Controller

If you find that the power controller in your High Performance Peripheral Cabinet just sits there and stares at you when you flip the breaker on, please check the two fuses on the Power Controller logic board prior to ordering (and waiting for!) a new Power Controller. These fuses are 2 amp ceramic 250V MDA-2, CONVEX P/N 253-000100-004

Dan Schoner

1.51.1 IDC Disk Error Script

The following script has been written to strip IDC related disk errors from the errorlog. This script is especially useful in locating media errors for slipping sectors. It also helps in isolating intermittent disk problems.
As can be seen from the script, it creates several different files to include a list of non repeatable errors, errors that have repeated more than once and all FSC errors.
The script is fairly well commented, but if there are any questions regarding its use, please contact the TAC.
Al,

cut here

```
#!/bin/csh
#
# read_errlog       Rev C.0
#
#           C.0:    strip partition and retry count off of line before
#                   determining singles and multiples
#           B.0:    initial release
#
if ($#argv != 1) then
      echo "Usage: $0 filename where              filename is an error log"
         exit
endif
set dir = "."
#
# read through an errlog file, pull out the FSC errors,
# and condense each error onto one line.
# Output and temporaries are in /log.
# FSC errors take two lines; 'i' keeps track. If a 'CCU' line does not start
# with 'FSC', then it gets put into a different file. This assumes that
# the second line of an FSC pair is always present.
#
fgrep '[CCU' $1 | awk -e 'BEGIN {i = 0} {if (i == 0) { if ($2 == "FSC") {for (j = 2; j <= NF; j++)
printf "%s ",$j ; i = 1 } else { print $0 > "NOTFSC" } } else {for (j = 2; j <= NF; j++) printf "%s
",$j ; printf " \n" ; i = 0}}' > $dir/Rawlist
cp NOTFSC $dir/NotFSC >& /dev/null rm NOTFSC >& /dev/null
# sort by errnumber, ccu, port, etc...
sort $dir/Rawlist > $dir/Errlist
# get a list of the FSC codes that appear
```

```
awk '{ print $2 }' $dir/Rawlist | sort -u > $dir/FSClist
cat </dev/null > $dir/Multiples
cat </dev/null > $dir/Singles
# get rid of partition and cnt
awk '{print $1,$2,$3,$4,$5,$6,$7,$8,$9,$10,$11,$12,$13,$14}' Rawlist > TmpRaw
# find any identical lines for each error type
foreach num ( `cat $dir/FSClist` )
   grep $num $dir/TmpRaw > $dir/Tmp1
   sort -u $dir/Tmp1 > $dir/Tmp2
   sort $dir/Tmp1 > $dir/Tmp3
   echo "" >> $dir/Multiples
   echo "sectors with multiple error" $num "are:" >> $dir/Multiples
   echo "" >> $dir/Multiples
   comm -13 $dir/Tmp2 $dir/Tmp3 | sort -u | tee $dir/Tmp4 >> $dir/Multiples
   echo "" >> $dir/Multiples
   echo "end of bad sector list" >> $dir/Multiples
   echo "" >> $dir/Multiples
   echo "" >> $dir/Singles
   echo "sectors with single error" $num "are:" >> $dir/Singles
   echo "" >> $dir/Singles comm -13 $dir/Tmp4 $dir/Tmp2 >> $dir/Singles
   echo "" >> $dir/Singles
   echo "end of bad sector list" >> $dir/Singles
   echo "" >> $dir/Singles
end
# a little cleanup
rm $dir/Tmp? $dir/TmpRaw
```

---

cut here

Please have a safe and happy Holiday season

2.1.1 Ultra problem

The rc.local file executes the rc.ultra file if it exists. No attempt is made to determine if there is an Ultra board installed in the system. If the rc.ultra file is executed and there is no Ultra board installed, a fatal convex error will occur and the machine will crash with a semaphore error. If the ultra board is removed for troubleshooting, the problem can be corrected by comment out the ultra reference in the /etc/rc.local.
Thanks to Kris Meier for this information
Regards,
Dave

2.1.2 idcfmt compatibility problem

There is a compatibility problem with idcfmt and the DB_idc that is loaded to /mnt/usr/lib on the spu from the IDC software V4.1 release tape or the Diagnostic Database V3.7 release tape.
In addition to disk geometry, the DB_idc file points to the location of the file RLL_2_7 which defines the test patterns to use during the format operation. When running idcfmt from SPU UNIX, the path to the pattern file (/mnt/usr/lib/DB_idc) is not resolved correctly and idcfmt aborts since it cannot find the pattern file. idcfmt operates correctly when run from ConvexOs in multiuser mode. If you have this problem, you will need to edit (on the SPU disk) /mnt/usr/lib/DB_idc. Change the file as follows:
> = Existing information in file DB_idc (DIAG_DB_REV V3.7)
< = Change to

.

```
# DB_idc - IPI DISK DRIVE PARAMETER FILE
(this file is abbreviated for simplicity)
#-------------------------------------------------------------------#
1 DKD-501 CDC_MPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 /usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /mnt/usr/lib/RLL_2_7
1 DKD-502 CDC_MPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 /usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /mnt/usr/lib/RLL_2_7
1 DKD-501 SEAGMPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 /usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /mnt/usr/lib/RLL_2_7
1 DKD-502 SEAGMPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 /usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /mnt/usr/lib/RLL_2_7 # . .
```

Regards Dave

2.2.1 New EFU/EDC Diagnostic

With the release of the new EFU/EDC's and their expanded functionality, new subtests have been added to the diagnostic misc4000 to test this new functionality.
The new functionality is to invalidate an entry in the data cache after encountering a parity error known as a 201/904. The new subtests verify this operation by setting parity errors and verifying that the entry has been invalidated.
These new test reside in 3.5 of the diagnostics and consist of class 3, 4 and 5 of misc4000. The new tests will only run on 3220 EFU's and 2219 EDC's. If other parts are installed in the system, then these subtests will not be executed on them.
Because of the way that the diagnostic is set up, it will only execute on a multi-headed system. If a head is disabled the diagnostic will test the head any way unless the older part is installed. This diagnostic will run on any 3220 and/or 2219 in the the cop.out file. If it is desired to run this diag on one head only, it will be necessary to install 2220/1219 boards in all other heads.
It has also been discovered that misc4000 will always fail subtests 50x when run on a standard C220. This is because the diagnostic was not written to consider a PIA in the system, but was written and tested on C240's with the PI2 installed. This failure will be corrected in the 3.6 release of diags. This diagnostic will run successfully on any wide body system.
The failure will appears as follows:

```
Subtest   500    0:00:02    failed
*****   Mon Dec 31 16:46:57 1990   *****
Test:    misc4000.t    1.7    Class: 5    Subtest: 500 1.7   Count: 1   Error: 0
Failed:     CPU0  RITA2-VAL2 connectivity test

 RITA_VAL:Dcache not invalidated
              CPU 0, page offset 0x0200 (RITA/VAL address 0x040),RITA 0 even
              gvalb 0x0, qvalb_synd 0x0, qvalc 0x0 qvalc_synd 0x0
              gvald 0x0, qvald_synd 0x0, qvale 0xf qvale_synd 0x0
```

As can be seen from this error, the error has occurred on the ebus. This is evidenced by the entry qvale 0xf. This failure should always be the same for the situation discussed earlier.
Al,

. . . continued on next page . . .

2.2.2

STC 196x Documentation Error

Please be aware of a typographical error in the STC 1960 Series Tape Subsystem F.E. Maintenance Manual.
In the first section, (FEMM) page 8-4 has paragraph 8.3.1.2 WRITE TEST PROCEDURE. The fourth line:
. . . according to the scheme defined in Table 5-1.
Is incorrect.
This line **SHOULD** reference Table 8-1, on the previous page.
Thanks to Stan Wood for pointing this out.
Dan Schoner

2.3.1 idcfmt and DB_idc

In a recent Technical Bulletin, Volume 2, Week 1, there was an article about an compatibility problem between "idcfmt" and "DB_idc". Well I want to take that problem one step further. It appears a similar problem existed in releases prior to V4.1 and now exists with V4.2 of the IDC software. In "DB_idc", located in "/mnt/usr/lib" on the SPU, and under V4.2 in "/usr/lib" on the JP, the path entry for "RLL_2_7" is "usr/lib/RLL_2_7". This poses a problem if, on the SPU your current path is not "/mnt" and on the JP your current path is not "/", "idcfmt" will start up, but then will error when trying to open the "RLL_2_7" file.
The following are two suggestions on how to get around the problem.
1. Make sure when you are on the SPU to be in "/mnt" and on the JP to be in "/" before executing "idcfmt".
2. Modify "/mnt/usr/lib/DB_idc" to show "/mnt/usr/lib/RLL_2_7" on the SPU and "/usr/lib/DB_idc" to show "/usr/lib/RLL_2_7" on the JP. With these files modified, you will not have to be in "/mnt" on the SPU or "/" on the JP.
See the examples below:

> = Existing information in file DB_idc
< = Change to.

```
# DB_idc - IPI DISK DRIVE PARAMETER FILE
 . . (this file is abbreviated for simplicity) .
#-------------------------------------------------------------------#
1 DKD-501 CDC_MPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /mnt/usr/lib/RLL_2_7
1 DKD-502 CDC_MPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /mnt/usr/lib/RLL_2_7
1 DKD-501 SEAGMPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /mnt/usr/lib/RLL_2_7
1 DKD-502 SEAGMPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /mnt/usr/lib/RLL_2_7 #
```

The above was for "/mnt/usr/lib/DB_idc" on the SPU.

. . . continued on next page . . .

2.3.1 idcfmt and DB_idc (continued)

```
# DB_idc - IPI DISK DRIVE PARAMETER FILE . .
.
. (this file is abbreviated for simplicity)
.
#-----------------------------------------------------------------#
1 DKD-501 CDC_MPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /usr/lib/RLL_2_7
1 DKD-502 CDC_MPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /usr/lib/RLL_2_7
1 DKD-501 SEAGMPI_EMD5 1635 50400 P 2048 ...
>2 DKD-501 BYTE 3000000 usr/lib/RLL_2_7
<2 DKD-501 BYTE 3000000 /usr/lib/RLL_2_7
1 DKD-502 SEAGMPI_S5L2 1635 50400 P 2048 ...
>2 DKD-502 BYTE 6000000 usr/lib/RLL_2_7
<2 DKD-502 BYTE 6000000 /usr/lib/RLL_2_7
```

The above was for "/usr/lib/DB_idc" on the JP.
Regards,
Chris Magargee

2.3.2 SYSTEM CONSOLE HANGS

It is possible for a system to hang with the /dev/console tty structure lock byte set. This basically makes the system console useless. The "console" program, on the spu, monitors for this and will attempt to unlock the console with the "lock_timeout" routine. This "timeout" is about 20 minutes on a C2 SPU.
Because of this long "timeout" count, there have been instances where systems and consoles appear to be hung and the system reset switch has been used regain control of the system. When the reset switch is used we loose valuable information that might assist in determining why the system hung.
If you have a system console that seems to have hung (ie. no response to <cr> <cntrlP> or <cntrlC>), please wait to see if the "lock_timeout" routine will return the console to the "spu>" prompt before hitting the system reset switch.

Dan Brenner

2.3.3 FMI 0079 and 0080

By this time you should have all the eproms needed to complete FMI's #0079 and #0080. If you find that you need additional eproms (for spares in stock), please send me some email and I'll arrange shipment to you. These FMI's were for ESDI and SMD controllers. Any questions, please call.

Thanks,
Mike Tweton

2.4.1 SPU Hangs

There have been many recent cases of spu hangs with the front panel display FF. An additional symptom is that when run the spu self test (spu1000) will hang at subtest 4 and indicate a power up interrupt.
These symptoms have, in all cases, led to a defective power supply and in most cases the power supply at fault had an inoperable fan. It appears that the heat build up by the defective fan causes the digital logic in the supply to hang in a manner that the SCM cannot handle.
In some cases it is possible to remove boards from the system and finally gain control of the spu, because the load has decreased sufficiently to be handled by remaining supplies. It is important to remember that the spu prompt can be reached with only the SP2/4 and PIA/PI2 installed in the system.
If encountering this problem, always approach it as a power supply failure and initially check for defective power supply fans.

Al,

2.4.2 Potential DAT problem

Please be aware of a potential problem with the DAT subsystem. This error has been observed once in-house and we have no indication that any field sites have experienced this difficulty. It is thought that this condition is brought about by a race condition of the DAT u-code, and we are working with Archive to identify the problem.
The following are the drive indications and the errorlog entries related to this problem:
The drive front panel will indicate a tape is present when no tape is loaded in the drive.
[CCU01@13:03:51] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
[CCU01@13:03:54] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
[CCU01@13:03:59] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
[CCU01@13:04:04] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
[CCU01@13:04:09] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
[CCU01@13:04:14] tc0: cmd TEST UNIT READY,status 0x8,error QUE_FULL or BUSY.
To correct this problem, load and eject a tape in the indicated unit.

Thanks to Paul Marshall for this information.

Dan Schoner

**********This condition was fixed by FMI0086**********

2.5.1 New Techtips and Revision Histories

The Techtips and Revision Histories Updates are back from the printers and will be shipped to the field during the next 2 weeks.
These are complete replacements of the Techtips and Revision Histories.

New or updated techtips included in this release:

POWER-006	C2XX	New (HC) Power Supplies
GEN-003	C2XX	C-2XX Matrix Charts
GEN-007	---	(FMI) History
GEN-011	---	Peripheral Configurators

Dan Brenner

2.5.2 UPGRADES TO C220's FROM C210'S

If you have a system with an 1128 or early 1156 backplane scheduled for upgrade to a C220, you should check to ensure there is a jumper between VCA P1-173 and VDA P1-173. This particular rework is required on all 1128 and 1156 backplanes, but during the early days of testing/shipping C210's the head A rework was missed on some systems. This could apply to cpu numbers 8255 and earlier.

Jerry

2.5.3 Reporting slipped sectors on IDC disks

Please remember to send e-mail to Chip Stroup (e-mail stroup@convex.com) when you have the occasion to slip a sector on an IDC disk.
It is particularly important that we are notified of sector slips. This information will be used to determine if the burn in time on Segate disk drives can be reduced.

Dave Muir

2.6.1 Diagnostic Failures

With the release of new products and the creation of new diagnostics, it is very important to understand that no diagnostic failure should be considered real until after mminit has been run. Only after mminit has been accomplished should a diagnostic failure be considered legitimate.
This has become particularly true of cpu diagnostics 4231, 4030 and 4233. As well as dev diagnostics 4540 (x.25) and dev_ultra.
There are no known failures with these diagnostics, but they have proven to have unique sensitivities which can cause erroneous errors if mminit is not accomplished prior to running them.
Recent mail from the field has hinted at known failures in diagnostics (cpu4030 and cpu4231) but these don't exist, except as a result of not performing a proper initialization prior to performing the diagnostics.

Al,

2.6.2 Crash Dumps

In order to clarify situations when crash dumps are required, I would like to make the following recommendations:
1)Crash dumps will never be of help when encountering a hard error. (i.e. ASP100, IPP300, etc.) A hwdump should always be done in these instances.In addition, a crash dump will be of no use against a 904 or 201 error. A dcache dump is the only useful tool in these cases. Since the release of 3.5 of the diag data base, the dcache dump is taken automatically in these cases and inserted in the errorlog.
2) I would also recommend that a hwdump be taken at the first occurrence of a system hang. This is because the crash dump resources are stretched very thin and because a hwdump can be analyzed in real time and help resolve the problem more quickly.
In many cases a hwdump and syshang can indicate whether a crashdump is necessary for future occurrence of the crash.
3) In all cases a crash dump should be taken when encountering any "Fatal Convex Unix" error. Or when a hwdump indicates a possible software failure.
Please remember that taking crash dumps for all failures will only result in a slower resolution of the problem and further taxing available resource.

Al,

. . . continued . . .

2.6.3 Power Supply Configuration

It is not possible to install more than three (3) -4.5 VDC power supplies in a C210 because the current share, as measured from pin 10 (IMON), will fall below 1 volt. This is because this threshold is called for in the current level of SCM microcode.
Any attempt to accomplish this will result in the error message "Too many supplies for configuration".

Al,

2.6.4 Disk Formatting

The overview section of the dev5130 diagnostics states that up to 12 disk drives can be formatted at the same time. Due to the memory requirements of the formatter, there in insufficient memory in the SPU to allow formatting of more than 10 drives at a time.
Thanks to Al Budriunas for bringing this to our attention.

Dave Muir

2.7.1 Sabre-5 Disk Drive Installation Note

When the new Sabre-5 disk drives are added to an existing system, installation of several new system files, diagnostic files and a sysgen are required. Please pay close attention to the release notes with the upgrade before proceeding. There are numerous steps that must be completed for a successful installation.

Dave Muir

2.8.1 FM0081-A

There has been a slight change made to FM0081. Instead of running the ground lead from P1-ASD-619 to P1-FUD-619, it is now run from P1-IPD-619 to P1-FUD-619. The ground at P1-ASD-619 is very close to a backplane stiffener and could cause a work space problem when trying to solder the ground lead into it, so the ground was moved to P1-IPD-619. This is change is being released in FM0081-A, which you will be receiving in the near future.

Regards,
Chris Magargee

2.8.2 Sabre5 Service Plan

The Service Plan for the Seagate Sabre5 SMD-E drive is being mailed (hardcopy mail) to the following Field Personnel:
Domestic: International: Tom Mucher John Parish Jan Plumb Jan Van Kats Horst Krenzke Richard Frisch Massimo Travella Shigeru Yoneyama Tim Gard Shawn Fuller
The above personnel are responsible for distribution within their own areas of responsibility.

Thanks
Dan Schoner

2.8.3 3480 and DAT tape diagnostics

With the release of 3.5 of the system diagnostics, the diag for DAT and 3480 tape drives have been merged into dev_vscsit. The diag v3480 has been deleted.
In the future, changes such as this will be documented in the release notes.

Al,

2.9.1 NEC Disk Drive Recovery

We have a new agreement with NEC as regards the 1.1GB Disc Drives.
If the drive fails at a "secure site" and the customer will not allow removal of the HDA from the premises, NEC will accept the unit for repair, replacement, etc., minus the HDA, if we specifically provide the following:

1. Customer Name.
2. HDA Serial Number.
3. All other component parts intact.

Drives returned from "secure sites" that meet the above criteria will be accepted as any fully intact unit would.

Thanks,
Brad Jones

2.9.2 Automatic dcache Dump Not Working

I have recently discovered that the automatic dcache dump for 201 and 904 crashes, is broken in 3.7 of the diagnostic database. This means that there may be no errors displayed in the dcache dump in the errorlog.
Because it was unknown that this utility was not working properly, it has caused some improper diagnosis of problems.
Please instruct customers to return to manual dcache dumps when encountering 904, or 201 related crashes. The proper command is as follows:

dcache -dh -c <head #> -e

This problem will be corrected in the 4.0 release.

Al,

2.10.1 C210 to C220 Upgrade - Fails Parallel Operation

When upgrading from a C210 to C220 and neither head will not work in parallel, but will each work individually; please verify the following:
a) Rev G backplane
b) EFU (Quite often a defective EFU will run in head B and not A)
c) EDC
If the above indicates no problems, then the problem is likely backplane related. If this is the case, nets below are the only nets (other than rev G) that will allow either head to function, but not both.

DCAFUBCYCLEL1	FUAFUBADDR0L<31..3>
DCAFUBMEREQL	FUAFUBADDR1L<31..3>
DCAFUBMOREQL	FUBFUAADDR0L<31..3>
DCBFUACYCLEL1	FUBFUAADDR1L<31..3>
DCBFUAMEREQL	IPIPDEADLOCK<7..0>
DCBFUAMOREQL	

TOTAL: 130 nets

One thing to keep in mind is that these nets (except IPIPDEADLOCK) are not terminated and can only be verified point-to-point and for shorts.
It is possible for these nets to be defective on, even, a new system as systems are not tested with both heads installed. Because of cost and time constraints both heads are not installed simultaneously and head A is slot tested. Because of this fact, these 130 nets will never be tested.

Al,

2.10.2 Sabre5 disktab Values

The disktab sample in the SEGATE SABRE5 SMD-E Service Plan, Para. 4.3 as shown is incorrect. Further pre-release testing has shown these values will not work correctly, and should not be used. The correct disktab will be shipped with the release software on system upgrades.

Thanks,
Dan Schoner

. . . continued . . .

2.10.3 C2 Fan Fail Sense Board Failures

******* WARNING *******

It is VERY important to understand that the rear door on a C2, with the cooling upgrade, should not be reinstalled while the system is powered up. This is because there is power applied to the circuit and can result in damage to the fan fail sense board. The action of plugging fans 9 & 10 in (rear door) is the same as trying to reinstall a board in the system with power on.

It is possible to unplug the fans in the back with power applied, but once removed, the door should not be reinstalled until the system is powered down.

Again, this warning only applies to standard C2's with the cooling upgrade installed. This can be verified by the presence of fans on the rear door.

Al,

2.11.1 Revision 4.0 Diagnostic Database and System Diagnostics

The 4.0 version of diagnostics and diagnostic_db has been released. This new release fixes some older problems as well introduces a few new things.
First off, this release will again allow the automatic dcache dump to function after a 904 or 201 crash. As I've said in previous mail, this has been intermittently malfunctioning recently.
This release will also fix the code associated with the scalar performance upgrade for both the 2220 and 3220 EFU's. This means that the adb patch for this will no longer be necessary.
In addition this release will contain the scan ring definitions for the new PI2, which will be released very shortly. This 3224 PI2 will fix the shortcomings of the 2224 and allow multiple PI2's to function is parallel operation. An FMI will be forthcoming to upgrade systems with multiple PI2's installed. There is no problem with the current PI2 in a system that does not have more than one installed.
As for new enhancements; The new diagnostic mem4100 is released to replace mem4000. This diagnostic has been completely rewritten and is very much superior to the old mem4000 diag. This new diagnostic will also allow the testing of the mcm3.
The scan definitions have been added for mcm3 as well as a new utility, mcm3_config. All iscn utilities have been modified to recognize the mcm3.

Al,

2.11.2 C2 Power System Troubleshooting

It has come to everyone's attention that the SCM's returned from the field as failed, in fact have the highest No Fault Found rate in Field Service Repair. This No Fault Found rate is 85% and appears to be in this condition because of a wide spread lack of understanding of the C2 power subsystem and how to troubleshoot a failure in this area. What follows is an attempt to explained clarify some major misconceptions in this area. First of all, it needs to be thoroughly understood that in the case of current sharing errors, in particular (i.e. 9x and Dx), the status code displayed is responding to a result instead of the original failure. In other words, when one supply's current share declines, another power supply's share increases to compensate. The status, almost invariably indicates the compensating supply as the failed device. In addition because of the removal of the ACPWROK line on the power supplies, the SCM is no longer able to determine that a supply has no output, or that the fan has stopped. All of these situations lead to some degree of confusion.
In spite of these shortcomings of the C2 power subsystem, with a little understanding and a few simple procedures it is possible to repair a failure in this area with minimal problems.
As almost everyone is aware, with the introduction of the slave/master relationship of the supplies, the adjustment procedure no longer calls for the removal of all of the boards, but can be done very simply with all boards installed. The procedure is as follows:

. . . continued on next page . . .

2.11.2 C2 Power System Troubleshooting

1) Power system down.
2) Remove 24VAC from SCM by removing cable at PDU If the system is a wide body (i.e. C240 type), remove ESM from the chassis.

NOTE

The SCM must be at least rev T for 130 version or be part number 411-000168-200.

It is also sometimes necessary to remove the cable from J14 on the C2 backplane. This is the SCM-SPU interface cable and can cause erroneous power readings. J14 can be located in the backplane drawing on page 5 of techtip CPU-013.

3) Place PDU in local.
4) Adjustment of shared supplies.
   a) Place neg. lead in ground and pos. lead in VEE for -4.5 and VTT for -2 VDC power supplies.
   b) Adjust master supply down to the point that there is no change, as indicated on the meter. This is the set point which is -4.4 VDC and -1.9 VDC depending on which type is being adjusted.

NOTE

Please do not adjust below the -4.4 VDC level, as this would indicate an improperly adjusted power subsystem.

   c) Adjust each supply in turn until the meter begins to increase, then adjust down until there is no more movement on meter. This sets all slaves to the slave set point value.
   d) Return master supply to proper position (-4.53 or -2.03).

5) Power system off.
6) Reinstall ESM or 24 VAC cable to the SCM.
7) Place PDU in Remote.
8) Power system up.

As stated previously, it is not uncommon for the SCM to indicate a failure with a supply that is compensating for reduced output of a failing supply. This quite frequently leads to some confusion about what to replace. In some cases, because of this less than accurate status, it is perceived that there must be something wrong with the SCM and it is replaced.

. . . continued . . .

2.11.2 C2 Power System Troubleshooting

This almost never corrects the problem, but does confuse the issue, slow the repair and generates additional costs for shipping and troubleshooting in Field Service Repair. The first step to be attempted when faced with a current sharing failure is to monitor the IMON line on the supply. This is located on pin 10 of the white molex connectors on the power supply. This IMON line indicates the current share of each supply in a DC level. The output is easily monitored by placing the black lead on pin 10 and the red lead on VTT on the backplane, if a -2 VDC supply, or VEE for the -4.5 VDC supplies. This is further explained in the tech tips under CPU-014. The indication on pin 10 should be that all slave supplies should be within 0.1 VDC of one another. The master should be approximately 0.3 VDC higher.
The next method to consider in this case would be to place the power controller in local position and monitoring pin 10 and turn the circuit breakers, on the power controller, off one at a time until there is little or no change in the meter display. This will indicate a supply that has little or no current output. Keep in mind that the breakers are numbered 1 thru 8 and 5-8 are -4.5 VDC supplies and 1 and 4 are -2 VDC supplies.
Another alternative, if the system is a C220, is to remove one head and leave the power controller in remote and toggle the supplies until you locate a supply that does not change the status from FF. This again would indicate a supply that is not contributing. One thing to keep in mind with this method, is that only 3 -4.5 VDC supplies should be turned on at a time, as the ucode will cause a failure because the current share will fall below 1 VDC. Thus causing a current sharing fault.

WARNING

I do not recommend this procedure, except as a last resort, as the multiple powering up and down can create new problems.

In the case of other failures it might be of help to simply verify that all power supply fans are spinning. Since the ACPWROK, pin 5, has been removed from most systems a fan failure or total supply failure will show up as a current share fault.
These are some helpful hints that may make troubleshooting the power subsystem a bit easier and decrease the number of No Fault Founds in the future.

Al,

. . . continued . . .

2.11.3 MCM3 memory

The MCM3 is finally nearing reality. This board will allow the existence of 2 GB memory systems and will replace the MCM2 in all future 1 GB systems.
The MCM3 will ship with any systems ordered with 1GB or greater memory, beginning April 1. And begin shipping with all C2's as the supply of existing MCM's is exhausted in mid to late May. Some of the specifics of the MCM3 are as follow:

1)The part number of the board is 410-002230-200.

2)The board uses a dmm (dual memory module) configuration similar to the mimm on the mcm2. The difference is that there are drams on both sides of the module.
There are 32 of these dmm's and will be field replaceable at this level.
The dmm's will come in sizes of 2MB, 4MB and 8MB

3)The iscn utilities mcm_scr and mcm_func have been modified to work with the mcm3.
I will detail these changes later.

4)The mcm3 is not compatible with the old 1213 memory boards.
They will be compatible with 3213 MCM's and MCM2's.

5) 4.0 of the diagnostics and diagnostic database is required.

6) The diag mem4100 will be the diag to test MCM3's and all other memory modules and will replace mem4000.

A Service Plan and other Technical Information will follow in the near future.
Al,

2.11.4 New PI2 Board

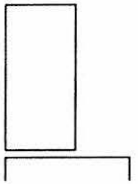
The respin of the PI2 is now being released. The part number for this new board will be 410-003224-200 and will replace the current 2224 boards in all new builds.
The PI2 was respun to improve the grounding configuration and to allow some parallel operation. However it will still not be recommended to stripe disks across two PI2's. This is because the way that the OS handles the windowing for the IO will cause a tremendous reduction in disk performance.
An FMI will be released soon to replace the 2224 PI2's on all systems that have multiple PI2's installed. This will not affect any system with single PI2's.
Al,

2.11.5 DAT Chassis Mounting Problem

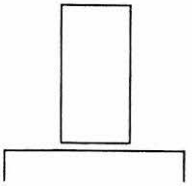
This instruction is needed to correct a minor assembly error that may have occurred on some Dat systems shipped to the field. If the front panel of the Dat Chassis will not fit on the Chassis when installed in the Cabinet the following procedure will need to be performed. The procedure should take 5 minutes and can be carefully performed while the unit is powered.

1. The Dat Drive itself has two sets of mounting holes. To check if your Dat Drive(s) are mounted correctly look at the front of the drive and note the following.....

Correct Mounting



Wrong



Note: The Dat Drive and the Mounting Bracket are FLUSH on the left-hand side of the drive, correct Config.

The "wrong" config. is offset by .375 to the right.

2. To install correctly, extend chassis, remove lid, unscrew the hardware holding the Dat Drive to the Mfab Strap across the top. (3) screws.
3. Unscrew the (2) bottom screws under the chassis that hold the bracket in place.
4. Unscrew the (2) screws holding the Dat Drive to the Bracket.
5. Shift the Dat Drive over to the left until the left side of the Dat Drive is flush with the left side of the bracket. Re-install the two screws thru the bracket into the DAT Drive.
6. Re-install the (2) screws from the bottom chassis into the mounting bracket.
7. Re-install the (3) screws holding the top of the Dat Drive to the Mfab strap and Chassis.
8. Install Front cover to RETMA Rail.

Thanks to Jim Day for the correct installation information.
Dan Schoner

2.12.1 Tech Bulletin Format

You may have noticed the ^L characters in the last tech bulletin. I am putting the formfeed character at the end of each page to facilitate printing the bulletin and manage the page breaks correctly. This helps with printing, but It causes some minor problems if you use less to view the document. Less does not seem to deal with formfeeds gracefully. If more is used to view the document, it seems to manage the formfeeds with no problems.

Regards,
Dave Muir

2.13.1 Printer Cables

There have been many questions regarding configurations of cables for printers attached to the V/Async printer port. Below is all information that would be necessary to interface a DataProducts, or Centronics printer to this port.

Data Products Printer cable
p/n 604-220001-001

P1	PAIR	P2
1	1	38
20		37
2	2	19
21		3
3	3	20
22		4
4	4	1
23		2
5	5	41
24		40
6	6	34
25		18
7	7	43
26		42
8	8	36
27		35
9	9	30
28		14
10	10	23
29		7
12	11	22
NC		NC
13	12	21
NC		NC

Jumper P1-17 to P1-36
P1 37 pin AMP connector
P2 50 pin "D" connector

Centronics Printer Cable
p/n 604-220002-001

P1	PAIR	P2
1	1	1
20		19
2	2	2
21		20
3	3	3
22		21
4	4	4
23		22
5	5	5
24		23
6	6	6
25		24
7	7	7
26		25
8	8	8
27		26
9	9	9
28		27
10	10	10
29		28
12	11	12
NC		NC
13	12	13
NC		NC

P1 37 pin AMP connector
P2 36 pin AMP connector

. . . continued on next page . . .

2.13.1 Printer Cables (continued)

The following is information relating to the pinout of the V/Async printer port.

Pin	Signal	Pin	Signal
1	DSTB	20	GND
2	PDAT<0>	21	GND
3	PDAT<1>	22	GND
4	PDAT<2>	23	GND
5	PDAT<3>	24	GND
6	PDAT<4>	25	GND
7	PDAT<5>	26	GND
8	PDAT<6>	27	GND
9	PDAT<7>	28	GND
10	DR	29	GND
11	NC	30	NC
12	RDY	31	NC
13	SLCT	32	NC
14	NC	33	NC
15	NC	34	NC
16	NC	35	NC
17	NC	36	NC
18	NC	37	NC
19	NC		

The vasync printer port provides a Centronics OR DataProducts interface. The type of interface is determined by the ioconfig entry for unit 16:

unit 16 type PRT-CEN selects Centronics
unit 16 type PRT-DAT selects DataProducts

The meanings and usage of the various control signals vary depending on the type of interface used.

PDAT	eight data bits
DSTB	data strobe, sent by vasync when printer data is valid.
DR	acknowledge, sent by the printer when it latches the data.
RDY	ready, sent by the printer when it is powered on, paper is loaded, and there are no errors.This signal is active-low in the Centronics interface and active-high in DataProducts mode.
SLCT	online, sent by the printer when RDY is asserted and the printer is online
GND	ground
NC	no connection

. . . continues . . .

2.13.1 Printer Cables (continued)

Standard Centronics
Printer Pinout

Signal Name	Signal Pin #	Return Pin #
DSTB*	1	9
DATA 1	2	20
DATA 2	3	21
DATA 3	4	22
DATA 4	5	23
DATA 5	6	24
DATA 6	7	25
DATA 7	8	26
DATA 8	9	27
ACK*	10	28
BUSY	11	29
Paper Empty	12	
SLCT	13	
AUTO FEED XT*	14	
SG	16	
FG	17	
SG	19-30	
INIT*	31	
ERROR	32	
SG	33	
+5	35	

Standard DataProducts
Printer Pinout

Input Signal	Pin	Output Signal	Pin
Data 1	19	Ready	22
Return	3	Return	6
Data 2	20	On Line	21
Return	4	Return	5
Data 3	1	Data	23
Return	2	Request	
		Return	7
Data 4	41	+5 volts	12
Return	40	(Test)	
Data 5	34	I/F verify	45,46
Return	18		
Data 6	43	Ground	11,27,39
Return	25		
Data 7	36	Not Used	31
Return	35		
Data 8	28		
Return	44		
Paper Inst	30		
Return	14		
Data Strobe	38		
Return	37		
IBOF	24,50		
Return	8,32		

2.13.2 Dual PI2 and IDC Stripes

Please Reference Weekly Technical Bulletin V2W11, paragraph 2.11.4. Additional testing reveals that IDC disk stripes that cross dual PI2's do NOT slow down disk transfer rates.

Regards
Dave Muir

2.13.3 3480/DAT tape driver error.

A problem was recently discovered version 2.0 of the 3480/DAT tape driver. It only affects systems that have two 3480 tape drives on the same SCSI formatter. Concurrent use of two 3480 tape drives on the same formatter may cause a cache controller error resulting in a system crash.
A patch is available from the TAC for sites that are experiencing the problem.
A fix for the problem has been identified and is being testing. All affected sites will receive the update to the the software when the ECN is released in the near future.
If you are using version 1.0 of the 3480 tape driver or version 9.0 of ConvexOs (version 1.0 of the driver is built-in 9.0) these problems will not happen.

Regards
Dave Muir

2.15.1 NEC Voltage Selection

Recently we have seen 4 occurrences of NEC disk drives randomly spinning down. The problem was traced to the voltage select switch on the drives being set to 240 volts instead of 120 volts. Setting the switch to 120 volts resolved the problem, with no other action required.
These drives had been functioning properly for more than 12 months when the problems showed themselves.

It is recommended that all NEC drives be checked during the next P.M.

Dan Brenner

2.15.2 Known Diagnostic Problems

The following are known C2 and Diagnostic related failures:

DEV 5130 -C 1, WHEN 2 DRIVES ARE CHAINED ON A CONTROLLER IT WILL NOT READ THE FLAW DATA CORRECTLY FROM THE DISK.

WITH THE -122 EPROM ON THE 168 SCM A BAD PS6 WITH NO DC OUTPUT REPORTS THE WRONG ERROR CODES AND DOES NOT SHUT THE SYSTEM DOWN.

CPX4000 -S 185 WHEN RUN MANUALLY FROM DSHELL WILL GET THE FOLLOWING ERROR MESSAGE: FAILED: INVALID PCM REFERENCE HARD ERROR CLEAR WHEN EXPECTED SET CPX BANK: A EVEN ADDRESS: 0X00000000 A SYSRESET CPUS -1 2 WILL FIX THE FAILURE.

FSCK MAY FAIL WITH MULTIPLE DISK DRIVES AND LIMITED MEMORY WITH V9.0 OS. ERROR MESSAGE, CACHE ALLOCATION ERRORS.

DEV 5130 ERROR REPORTING OF MISSING FLAW INFORMATION IS INCORRECT . ALSO FORMATTING MORE THAN FIVE DRIVES AT A TIME IS NOT POSSIBLE IF ERRORS ARE ENCOUNTERED DURING THE FORMAT ROUTINE.

MULTIPLE 3480'S CRASH THE SYSTEM WITH 2.0 SCSI SOFTWARE WHEN A TAPE IS EJECTED WHILE READING ANOTHER.

THE 'COMMREG' UTILITY NEEDS TO PRINT BOTH COPIES OF THE LOCK BIT. (FROM THE CUO AND CUE) PROBLEM IN 4.0 DIAGS.

. . . continued . . .

2.15.2 Known Diagnostic Problems

IN DIAG 4.0 CPU4233 SUBTEST 521 OCCASIONALLY HANGS. WHEN 4 HEADS JOIN, THE LAST HEAD TO JOIN CANNOT RECEIVE THE THREADCOUNT BECAUSE THE OTHER 3 ARE PASSING IT AROUND IN THE IDLE LOOP. THIS IS NOT A PROBLEM UNDER OS.

DIAG 4.0 CPU4233 SUBTEST 571 INTERMITTENTLY FAILS WITH 3220 EFU's INSTALLED DISPLAYING A REGISTER DUMP.

Al,

2.15.3 Boot Problems After Upgrade to ConvexOS 9.0

Some sites have recently experienced difficulties during the upgrade to ConvexOS V9.0. You may see a large and long list of caching errors in several circumstances: booting to multi-user, or running preen(8), or running fsck(8) on a stripe.
The problem is that the system doesn't have enough memory and swap (that it knows about). When it tries the preen or the fsck, it runs out of memory and gives the caching errors. This may also occur when running the clrinodefld(8) script when upgrading to ConvexOS V9.0. (clrinodefld is much like preen; however, its output is redirected to /dev/null and error messages may not appear.)
This can happen on machines with low memory and lots of disk (there are no numbers available on what defines "low" and "lots" here; sorry). This can happen to both C1s and C2s, with and without stripes.
The work-around, as documented in the "Read Me First" attachment to the ConvexOS V9.0 Release Notes (dated December 10, 1990) is to move the line "/etc/swapon -a" to be immediately before the line "if [-r /fastboot]" in the system /etc/rc file.

Josh Simon

2.16.1 Revision 4.0 Diags

It has been discovered that the softlog in 4.0 of the diagnostics does not decode the board location, in the address, properly. This means that the only way to determine the board causing soft errors is the address reported in the errorlog. Unfortunately soft errors are not always reported in the error-log.
This will be corrected in the next release of diagnostics.

Al,

2.16.2 Auto-reboot Information

Auto-Reboot is a new utility that exists with the combination of 9.0 OS and 3.7 of the diag database. This utility is to allow the automatic reboot of the system if it should crash for anyone of 3 different causes.
The auto-reboot facility is controlled by the spu file /mnt/os/reboot_control. The options available in this file are:

1) reboot_timeout
2) reboot_on_panic
3) reboot_on_hang
4) reboot_on_misc
5) hangmntr_options

The reboot_timeout entry controls the time the system will wait for operator intervention, after a crash, before the system reboots automatically. The default for this is 10 minutes.
The next 3 entries can have the value of "yes" or "no" i.e.
reboot_on_panic=no reboot_on_hang=yes reboot_on_misc=no
These entries will enable or disable an auto-reboot after one of these conditions occur. The "reboo-t_on_misc" covers all other reasons for a crash not covered by panics or hangs.The default for all of these is no.
The entry "hangmntr_options" is a utility that attempts to detect system hangs and crashes the system when one is detected.
Two switches exist with this entry:
-b minutes = time after booting before running checks
-t minutes = time clock must be stopped before reboot
An example would be; hangmntr_options="-b 20 -t 5"
The -b switch is set to allow booting time for the system. This option does not normally require an entry as the default is as above.
Al,

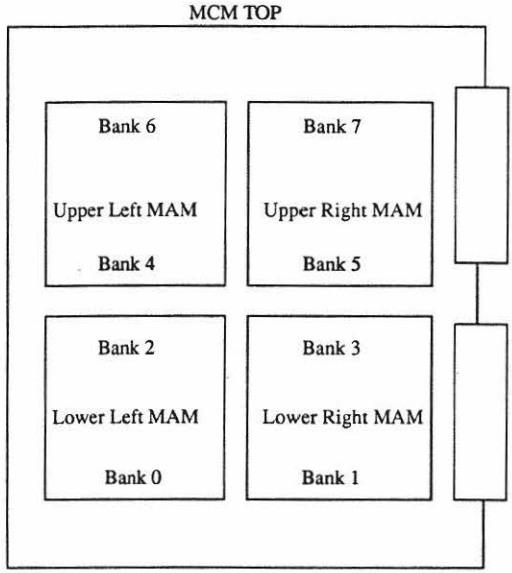
2.16.3 IDC Power Controller Fuses

As a result of the recent field survey, concerning the 2 amp fuse in the High Performance Power Controller, it has been determined that the current fuse does not perform properly under heat. Therefore this fuse will be replaced with a 3 amp regular fuse.
This new fuse will be installed in all new builds.

Al,

2.16.4 MCM MAM Location

The following is the proper orientation of MAM's and Banks on the current MCM's.



Al,

2.16.5 VMEbus Sabre5 SMD disk Drive Service Guide.

In the VMEbus Sabre 5 SMD disk Drive Service Guide, Figures 1-2, and 1-3 on pages 1-4, and 1-8 respectively, illustrate the position of various drive jumpers, switches, and LED's that should be checked prior to drive installation. While Figure 1-3 accurately shows the ON/OFF positions for all the I/O switches, Figure 1-2 (the Control board) does not. Because of this fact PLEASE ensure that you consult the tables for the correct switch settings.

Kelvyn Gipp

2.16.6 MCM3 Information

The MCM3 will soon be available and will allow physical memory to reach 2GB. The MCM3 will be populated with up to 32 DRAM Memory Modules of different sizes. There will be no performance increase for the MCM3, but will be cheaper and allow the increased memory sizes.

The following are the specs and prerequisites for the MCM3:

PART NUMBERS

MCM3 (unpopulated)	410-002230-200
2MB DMM	411-000204-200
8MB DMM	411-001204-200

4MB DMM will only be manufactured if absolutely necessary.

PREREQUISITES

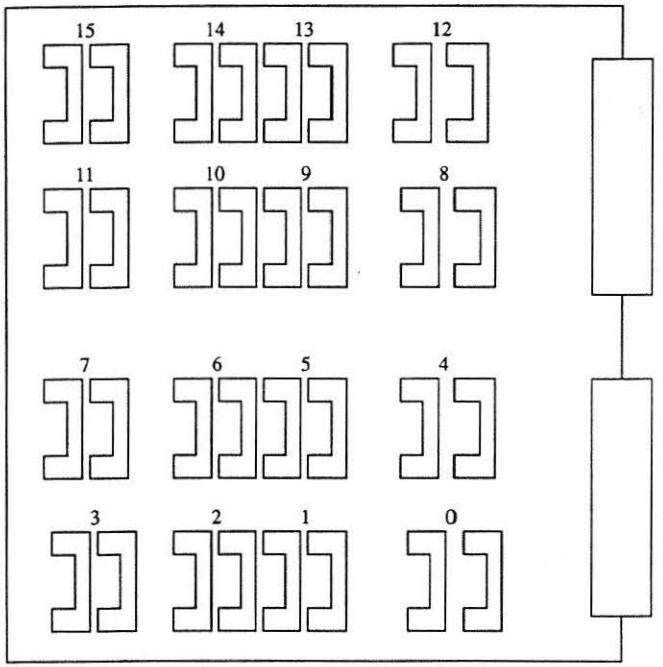
1) 4.0 Diagnostics
2) 4.0 Diagnostic Database
3) Diagnostic mem4100
4) CUO 6221 and CUE 6222 for 2GB system
5) CUO 3221 and CUE 3222 for 1GB system
6) CPX 6201 for 1GB, or 2GB standard C2 system

The MCM3 can co-exist in the same system as either the 3213 MCM, or the MCM2. It cannot, however, be installed with the 1213 MCM's.
The MCM3 can exist with only 8 DMM's (DRAM Memory Module) installed. This would include at least one DMM installed in each logical bank.
The documentation for the MCM3 will be chapter 4 of the C3400 "Theory of Operation" Manual.
The iscan utilities mcm_func and mcm_scr have been modified for use with the MCM3.

See following page for a graphic representation of the MCM3

2.16.6 MCM3 Information (continued)

MCM3 PHYSICAL BANK LOCATIONS
(Each bank consists of 1 pair of DMM's)



Logical Bank		
	0 corresponds to	Physical Bank 0 & 8
	1 corresponds to	Physical Bank 1 & 9
	2 corresponds to	Physical Bank 2 & 10
	3 corresponds to	Physical Bank 3 & 11
	4 corresponds to	Physical Bank 4 & 12
	5 corresponds to	Physical Bank 5 & 13
	6 corresponds to	Physical Bank 6 & 14
	7 corresponds to	Physical Bank 7 & 15

2.17.1 IDC Cable Problem

It has been discovered that the IDC cable has, in some instances, been trimmed improperly at the backplane connector. This can allow the cable to short to the 5th column of pins left exposed after the connector is installed. This shorting can cause any type of failure ranging from "loadccu time-out" to failure of the drives, on that port, to attach during autoconfig at boot.

This problem appears to be wide spread, as there are no instructions requiring the cable to be trimmed flush with the connector head. Manufacturing is studying the situation and a correction will be available soon. In the mean time, a work around is to install a piece of electrical tape over the exposed cable end. This will prevent the cable from making contact.

The figure below shows the relationship of the cable to the pins on the backplane. The short will occur between the side of the connector and column 5.

```
1 234 5
 ___
 |...|
.|...|.
.|...|.
 |...|.
.|...|.
.|...|.
.|...|.
```

Achim Hoffman

2.17.2 IDC Troubleshooting

The following are some useful hints to be used when installing IDC's:

1) Instead of wasting time with the boot process, when troubleshooting "loadccu timeout" problems it is possible to run the utility loadccu from the spu and save a little time. The procedure is as follows:

   a) pqutil -I
   b) loadccu -<ccu#> /mnt/os/idc

.....continued on next page.....

2) On rare occasions, it has been found that a differential CCU (IDC, TLI, HSP, etc.) will not will not function is some CCU slots. If a failure is encountered that can not be explained, it might help to try the IDC in another slot.

3) Because of the reduced size of the cable on port 3, some of the control lines actually pass to the bulkhead via the cable on port 2. This means that a failure on port 3 only, can actually be caused by a failure of the cable on port 2.

4) It is possible that excess cable on the backplane connector can short to pins in column 5 on the backplane. Please see entry in this bulletin for further details.

5) It is still necessary to locate IDC entries at the bottom of the ioconfig problem. If this is not done, it will cause memory allocation problems.

6) It is possible to boot a system with no drives attached to an IDC, if these drives are physically removed from the ioconfig file. This will enable the IDC and ports to pass the probe and attach portion of the autoconfig. This will also work with all cables removed from the backplane. This is useful info when trying to determine if a problem is slot or cable dependent.

These tips can be used to make troubleshooting IDC installation failures much easier and quicker.
Al,

2.17.3 IDC Performance

It is important to understand that performance on disks can be increased by increasing the block/frag size of the file system. This serves to allow more data to be transferred during each operation.

The default, for instance, with IDC is a 16k block size with a frag size of 2k. This works fine for partitions with many small files, such as root and usr, but actually decreases performance when used with scratch or data file systems.

The recommended size for blocks on IDC is 64/8 and although this does affect disk volume slightly it increases performance greatly. This means that 64k should be transferred on a request, as opposed to the default of 16k.

This should be explained to customers when performance issues are discussed.

This is discussed in far more detail in chapter 4 of the manual "Managing ConvexOS: Configuration Guide".
Al,

2.18.1 IPI disk drive bad sectors

There have been questions about the maximum allowable number of defective sectors on the IPI disk drives.

Most of the disk drives received have between 100 and 300 flaws in the manufactures flaw map. however, the maximum allowable number of flaws is 574. No drives will be accepted from the vendor by Convex Quality Assurance that exceed this number of flaws. As a result of incoming inspection, no drives will be shipped to the field with more than the maximum number of flaws.

In addition, no drives that are ordered by model number will be shipped without being formatted. It should not be necessary to format drives as part of the installation.

If you find it necessary to format any disk drive during an installation, please contact the TAC with the serial number of the drive and the symptoms the drive exhibited before being formatted.

* Dave Muir *

2.18.2 IDC - idcfmt program

When running the idcfmt utility from the SPU, the verify command will not work if the disk drive under test is write protected. When idcfmt is run from the OS, the verify command will operate with the drive write protected.

This problem will corrected in a later release of the idcfmt utility.

* Dave Muir *

2.18.3 SPU Unix errors 108 & 109

Since the 3.4 release of diagnostics, it has been possible to intermittently encounter "spu unix 108 and 109" errors when running spu4000 or performing cop -f.

These errors are soft and random and should be ignored when encountered.

This problem has been too elusive, up to now, to correct, but it is possible that 4.0 has increased the frequency of these messages.
Al,

2.18.4 Sabre5 Part Information

As CONVEX's utilization of the Seagate Sabre5 series product increases, there exists an opportunity to save CONVEX some money by working smarter AND reduce customer stress in the event of a disk drive failure.

The Seagate products currently offered by CONVEX are:

204-000016-200	Seagate ST81236K (or model #97229-IIG or model #PA8Y2A) 6.0 Mb/sec IPI Interface (DKD-502)
204-000017-200	Seagate ST81154KT (or model #97209-12G or model #PA8R2A) 3.0 Mb/sec IPI Interface (DKD-501)
204-000021-200	Seagate ST81236J (or model #PA8N2A) SMD Interface (DKD-281)

These drives have proven to be quite reliable, and are exhibiting lower HDA failure rates than previous offerings. Since all of the above drives are of the same Sabre5 family, there exists an opportunity to repair a failed drive rather than replace the entire unit. We can remove some of the customer pain associated with a disk drive failure by troubleshooting and repairing logic board and power supply failures at the customer site. Field Logistics stocks the optional Seagate Sabre5 Status/Control Panel to assist in trouble- shooting these drives. Refer to Tech Tip Disk-017 and the Seagate Sabre Disk Drive Maintenance Manual (CONVEX P/N 900-000421-005) Section 2 for diagnostic instructions.

CONVEX Logistics will stock the following spare parts for Seagate Sabre5 series products:

Seagate P/N	CONVEX P/N	Description & Applicability
50706xx*	204-000016-010*	Power Supply (ALL Sabre5 products)
450706xx	204-000017-002	Power Supply (SMD & 3.0 Mb/sec IPI ONLY)
544041xx	900-000343-001	AWRX Operator Panel(ALL Sabre5 products)
543977xx	900-000341-001	CVZX Status/Control Panel (ALL Sabre5)
544165xx	900-000066-001	AXYX Control Board (SMD & 3.0 IPI)
544201xx	900-000346-001	GYBX Control Board (6.0 Mb/sec IPI ONLY)
543945xx	900-000067-001	LVRX-3 Dual Channel I/O Board (SMD ONLY)
54421755>58&60	900-000344-002%	LYBX I/O Board - 8 switch board (replaces 8 or 9 switch IPI)
54421759	900-000344-001	LYBX I/O Board - 9 switch board (replaces 9 Switch IPI ONLY)

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* Initially, CONVEX will stock ONLY the 204-000016-010 Power Supply. If a 204-000017-002 Power Supply is needed for a 3.0 Mb/sec or SMD drive, this power supply (204-000016-010) can be utilized.

% CONVEX P/N 900-000344-002 can replace EITHER 8 or 9 switch IPI I/O boards. CONVEX P/N 900-000344-001 CANNOT replace the 8 switch IPI I/O board due to the smaller size of the access cutout on the Rear Panel. Refer to Tech Tip GEN-011 for switch position settings. The ONLY difference in the setting of the switches is switch number 9 - on the 8 switch I/O board, switch 9's functionality is accomplished by a jumper - all other switch assignments are exactly the same.

Thank You Very Much
-- Dan Schoner

2.19.1 Mag Tape errors

The "tar" utility has only one error message that is printed when a error occurs during write operations, regardless of the type of tape error that has occurred. The error message is:

tar: Write error : EOT seen.

This error message will be printed on any hard error that is experienced during the writing of a tape.

Since soft tape errors are not placed in the system errlog, so you may have marginal operation of the tape drive, without being aware of it, until you get hard failures during tape operations.

Regards
* Dave Muir *

2.20.1 Diagnostic Release 4.1

Diagnostic Release 4.1 has now been signed off. This is the prerequisite for installation of MCM3's and most fixes are specifically for operation and testing of MCM3's. However this release also fixes the softlog bug that prevented 4.0 from reporting the location of a memory error. This fix is important and should be considered for replacement at all sites with 4.0 diags loaded. The following are a list of fixes in 4.1:

errintd	The portion of errintd that logs soft errors in /mnt/softlog has been fixed. The 4.0 version could not find some soft error addresses in MCM3's, and in any case would log the addresses incorrectly.
hard_logger	The hard logger has had its routine that searches the MCM3 win queue for failed addresses & syndromes fixed. The 4.0 version had an approximately 50% chance of not being able to find the address and syndrome of any hard or soft error in the win queue.
mcm3_config	The 4.0 version sometimes incorrectly configured the MCM3 boards. This has been fixed.
mminit	4.0 mminit was unable to size memory in a system that contained any MCM3's that weren't fully populated. This has been fixed.
sysreset	These have been updated to support the new 6201 CPX and the 6222 CUE/6221 CUO. This is especially important concerning the 6222 CUE/6221 CUO, since these need to be configured properly to work as a 2G CU pair (it is possible to make the 6222 CUE/6221 CUO behave as a 1G 3222 CUE/3221 CUO pair).
cpu4010	This has been fixed to test the complete range of R&M bits for a 2G system.
cpu4241	These have been updated to support the new 6201 CPX and the 6222 CUE/6221 CUO. No new functionality was changed or improved.
cpx4000	This was updated to test the complete range of R&M bits for a 2G system.
mem4100	The 4.0 version of mem4100 would not work properly on systems containing MCM3's with unpopulated DMM's. In addition, subtest 5110 (address = data) contained a bug that would cause it to fail. These have been fixed.

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misc4000 This was updated to support the new 6201 CPX and the 6222 CUE/ 6221 CUO. In addition, it should be completely functional on C210/C220 systems (that is, ones with EFUs/EDCs).

pi2_4000 These have been updated to support the new 6201 CPX and the 6222 CUE/6221 CUO. No new functionality was changed or improved.

Al,

2.20.2 MCM-3 Memory Information

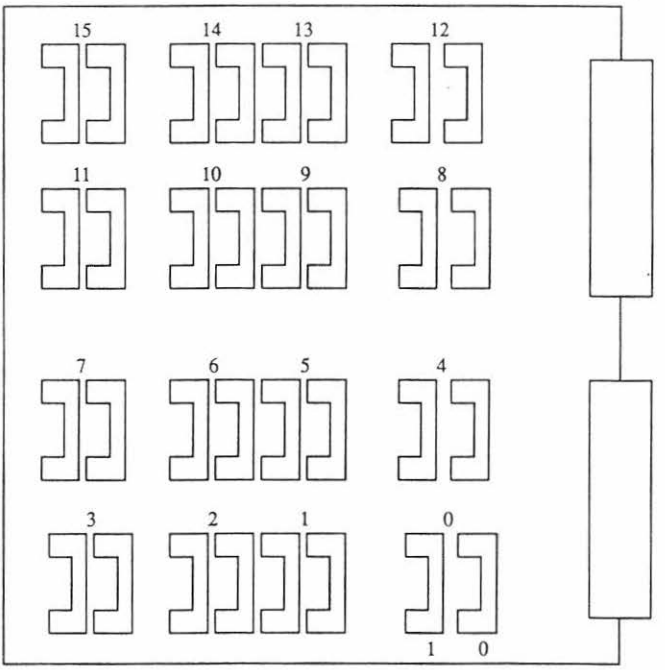
The MCM3 is finally released and the first 2GB memory system will ship on 17 May 91. This document is intended to detail all necessary technical information concerning the MCM3. This document also replaces a previous MCM3 Tech Bulletin that was issued.

The MCM3 offers CONVEX a less expensive memory board and the capability to install up to 2GB of physical memory in all C2 products. There is no performance enhancement with the MCM3.

Like the MCM and MCM2, the failed component location can be determined from the memory address. The same basic rules apply, but is somewhat more complex because of the concept of physical and logical banks. To understand this concept, keep in mind that there are 16 physical banks on the MCM3 and it takes 2 physical banks to make up one (1) logical bank. This can be seen from the drawing and table below:

.....continued on next page.....

MCM3 PHYSICAL BANK LOCATIONS
(Each bank consists of 1 pair of DMM's)



.....continued on next page.....

LOGICAL BANK	CORRESPONDING PHYSICAL BANKS
0	0,8
1	1,9
2	2,10
3	3,11
4	4,12
5	5,13
6	6,14
7	7,15

As can be seen from the table and drawing above, the physical banks that produce the actual logical bank reside on different halves of the MCM3. For example; Logical Bank 0 is made up from physical bank 0 which is in the lower right corner of the MCM3 and physical bank 8 which is the same position on the top half of the board. It should be noticed that there are two DMM slots for each physical bank.

One other concept that is different is the fact that the MCM3 can be 1/4 or 1/2 populated. In other words you can place 8 or 16 DMM's on the board, rather than the 32 for a fully populated MCM3. To accomplish this for 1/4 populated, it is necessary to install one (1) DMM in each physical bank 0-7. In addition it is important to know that the first DMM slot is on the right, as shown in the drawing above. Note that physical bank 0 has DMM slots labeled 0 and 1.

To produce a 1/2 populated board the same rules would apply, except that one DMM would be placed at location 0 in all 16 physical banks.

Because the board has so many configurations the addressing more complex than in the past. Because of this complexity, it will be necessary to give several variations on this representation.

1Mb (256kx4) DRAMS
1/4 Populated

MCM Pairs	Physical Memory	Pair Select	Row Select	Logical Bank	Even=0 Odd =1
1	32MB	-	28	5..3	2
2	64MB	6	28	5..3	2
4	128MB	7,6	28	5..3	2

.....continued on next page.....

1/2 Populated

1	64MB	-	25,24	5..3	2
2	128MB	6	25,24	5..3	2
4	256MB	7,6	25,24	5..3	2

Fully Populated

1	128MB	-	28,25,24	5..3	2
2	256MB	6	28,25,24	5..3	2
4	512MB	7,6	28,25,24	5..3	2

4MB (1Mx4) DRAMS
1/4 Populated

1	128MB	-	28	5..3	2
2	256MB	6	28	5..3	2
4	512MB	7,6	28	5..3	2

1/2 Populated

1	256MB	-	28,31	5..3	2
2	512MB	6	28,31	5..3	2
4	1GB	7,6	28,31	5..3	2

Fully Populated

1	512MB	-	29,27,26	5..3	2
2	1GB	6	28,27,26	5..3	2
4	2GB	7,6	28,27,26	5..3	2

Pair Select - Board Pair experiencing problem
Row Select - Indicates binary weight of DMM location
Logical Bank- Binary weight of logical bank 0-7
Even/Odd - Indicates Even or odd board in pair

.....continued on next page.....

To figure the location of the failed DMM think of the logical bank in terms of both physical banks combined. This produces DMM locations 0-3 with 2 and 3 residing in the upper physical bank. Note Drawing above for numbering of DMM locations in physical bank 0 and 8.

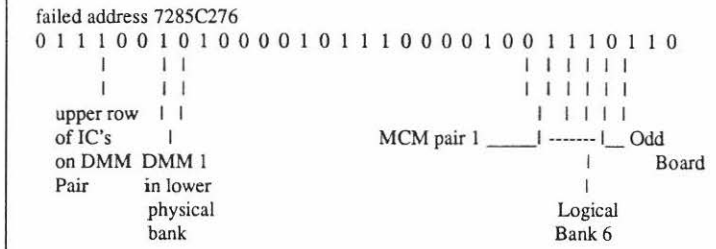
In the case of the 1/4 populated board, bit 28 just indicates the side of the DMM in error, where a 1 indicates the upper side. Keep in mind that each DMM consists of 10 DRAMs on both sides and each side is considered a row.

For the 1/2 populated board bit 24 will indicate whether the Failed part is in upper or lower physical bank and bit 25 indicates the side. For the 4MB DRAMS 28 and 31, respectively, are used for the same reference.

For fully populated boards with 1MB DRAMs bits 24 and 25 will give the location of the DMM and bit 28 will be the failed DMM row. For the 4 MB DRAMs it'll be bits 26 and 27 for the DMM slot and 28 for the DMM row.

The following example may clarify the explanation:

The example is for a system with 4 board pairs of fully populated MCM3's with 1MB DRAMs installed:



PART NUMBER

Unpopulated MCM3	410-002230-200
2MB DMM	411-000204-200
8MB DMM	411-001204-200

* 4MB DMM will only be manufactured if absolutely necessary.

.....continued on next page.....

PREREQUISITES

1) 4.1 Diagnostics
2) 4.0 Diagnostic Database
3) Diagnostic: mem4100
4) CUO 6221 and CUE 6222 for 2GB system
5) CUO 3221 and CUE 3222 for 1GB system
6) CPX 6201 for 1GB, or 2GB standard C2 system
7) PI2
   a) 1224 rev E
   b) 2224 rev H
   c) 3224 any rev

The MCM3 can co-exist in the same system as either the 3213 MCM, or the MCM2. It cannot, however, be installed with the 1213 MCM's.

The documentation for the MCM3 will be chapter 4 of the C3400 "Theory of Operation" Manual. The iscan utilities mcm_func and mcm_scr have been modified for use with the MCM3.

Al,

2.21.1 Formatting Unformatted IPI Disk Drives

There is a problem encountered when using the idcfmt utility to format a un-formatted IPI disk drive from the OS level.

During the boot, a virgin disk will report a lot of errors during the probe and attach phase (during autoconf). This is due to the machine trying to read the topology map which is not present on a virgin disk.

The work-around for this problem is to turn off the autoconf timeout in /mnt/os/boot. Change the line "autoconf ..." to "autoconf -t ..." when you know that you will be booting with a virgin IPI disk. You will get many errors during the boot (around 30 to 40 per drive), but the boot will complete.

The line in /mnt/os/boot should be changed back to the original form after the drives have been formatted to prevent possible problems during the boot process at a later time. A formal fix will be incorporated in the software in a future release.

Dan Schoner

2.22.1 CONVEX Maintenance Documentation (C200 Series) Error

There is an error in the above mentioned documentation. Refer to the Removal/Replacement manual, 081-001030-201, Rev.1, February 1989. Section VI.4 pages 65, 66 and 68 contain an incorrect figure. The orientation of the backplane pins is incorrect. The text of the instructions for removing and installing backplane pins is correct. These figures will be corrected in an update to the manual.

Regards
* Dave Muir *

2.23.1 dev4300 st206 failure.

dev4300 may fail this, or other internal loopback tests, if any "intelligent" peripheral is attached to the Systech panel when the when the diagnostic is executed.

During internal loopback tests, the Systech controller's data and status lines are not disconnected from the external comm port. Data going out on the port may cause an attached peripheral to return data to the port. This will result in a diagnostic failure, since the data and status received will not be what was expected by the diagnostic.

Thanks to Don Conover for bringing this problem to our attention.

* Dave Muir *

2.24.1 PETS version information

As a reminder, PETS version 2.2 will encounter wrong answers in subtest 30. This can be solved by removing test 30 from the tests script under the PETS directory. In addition version 2.2 will not execute with version 4,0 of the diagnostics and database.

Both problems can be resolved by running version 2.3 of PETS exclusively. This version has been released since Oct.

Al,

2.24.2 mem4100 intermittent subtest failure

The new memory diagnostic mem4100 will intermittently fail at subtest 51xx on a three headed system and will always fail on a three headed system with only 2 pair of memory boards.

This problem will be solved with version 4.2 of diagnostics.

Al,

2.24.3 Memory pairs vs Heads in a c220i system

In the past it has been standard practice to ship at least one pair of memory boards for each head in a system. This is a good practice as having fewer pairs than heads can result in system crashes, particularly "Fatal CONVEX Unix" errors.

In this light it should be pointed out that the 220i systems, which are the expanded I/O systems, use memory port D for the additional PBus's, v and w. For this reason this system should be considered as having an additional head on the D port. This means that the system memory should be configured the same as that for a 3 or 4 headed system.

This should be explained to sales people so that these "i" systems are not sold with a deficiency in memory.

Al,

2.24.4 MCM3 and PI2 minimum Revision Level

As explained in an earlier Tech Bulletin, on the MCM3, the minimum rev of PI2 is E for the 1224 and H for the 2224 PI2. If the PI2 does not meet this requirement, "write data parity errors" will result. If a system with MCM3's installed exhibit this failure, the PI2 rev level should be considered.

Al,

2.24.5 Time Of Century (TOC) ECN on PI2.

An ECN has recently been installed on the PI2 to correct a TOC problem in the C2 systems. The ECN changes the revision level of the 410-002224-200 to revision J. This resolves a problem with system crashes when accessing the TOC from the I/O subsystem.

The modified PI2 must be installed in the PIY slot if the customer wishes to access the TOC from the I/O subsystem.

Thanks to Dennis Maloney for this information.

Regards
* Dave Muir *

2.25.1 DKD-281 disktab entries for Saber5 Disk Drives

There has been some confusion about disktab entries for the DKD-281 disk drives.

Here's the history of the DKD-281 disktab - UNDER NO CIRCUMSTANCES should sections 1 or 2 be in the field!!

```
================================================================================
Pre-Sabre5 SMD
================================================================================
dkd-281|DKD-281|VCDC9720G|CDC 9720 on VME:\
:ty=winchester:se#512:ns#83:nt#15:nc#1635:rm#3600\
:pa#100736:ba#8192:fa#1024:\
:pb#407040:bb#8192:fb#1024:\
:pc#2023040:bc#65536:fc#8192:\
:pd#102016:bd#8192:fd#1024:\
:pe#611200:be#4096:fe#512:\
:pf#202880:bf#4096:ff#1024:\
:pg#916224:bg#4096:fg#512:\
:ph#598784:bh#4096:fh#1024:
================================================================================
Sabre5 1.0
================================================================================
dkd-281|DKD-281|VCDC9720G|CDC 9720 on VME:\
:ty=winchester:se#512:ns#83:nt#60:nc#1624:rm#3600\
:pa#100736:ba#8192:fa#1024:\
:pb#404608:bb#8192:fb#1024:\
:pc#1952528:bc#65536:fc#8192:\
:pd#100736:bd#8192:fd#1024:\
:pe#606208:be#4096:fe#512:\
:pf#201600:bf#4096:ff#1024:\
:pg#908800:bg#4096:fg#512:\
:ph#595072:bh#4096:fh#1024:
```

.....continued on next page.....

Sabre5 1.1

```
dkd-281|DKD-281|VCDC9720G|CDC 9720 on VME:\
:ty=winchester:se#512:ns#83:nt#60:nc#406:rm#3600\
:pa#100736:ba#16384:fa#2048:\
:pb#403380:bb#16384:fb#2048:\
:pc#2021880:bc#65536:fc#8192:\
:pd#100736:bd#16384:fd#2048:\
:pe#602580:be#16384:fe#2048:\
:pf#201600:bf#16384:ff#2048:\
:pg#911340:bg#16384:fg#2048:\
:ph#595072:bh#16384:fh#2048:
```

Dan Schoner

2.26.1 DKD-501 and Striped "C" Partitions

A subtle reminder to all IDC DKD-501 users.

While Convex OS 9.0 and above corrects entries in /etc/disktab to allow customers to utilize these drives in stripped file systems, an additional change is required should the customer desire two "c" partitions to be stripped together. The "pc" must be changed to the following value:

:pc#524160: unchanged : unchanged :\

Once the new value has been inserted, run "newst" as you would normally.
If you use these drives on an 8.0/8.1 system, please consult the allfe mail that was distributed on 12 Oct 90, titled "IPI Disk Drive Partitions"

Kelvyn

2.26.2 Crashdump Failures with IDC and TLI

It appears that a problem exists with some IDC's and TLI's that prevent a crashdump from running on the system. Basically the crashdump will abort when trying to dump one of these modules. The crashdump will usually abort with a "spu unix 109" error.

Right now the work around for the problem is to remove the IDC, or TLI from the ioconfig file and reinitiate the crashdump.
This problem is being investigated and when a solution is found the field will be notified. This problem does not affect all IDC's, or TLI's and so, should be handled on a case by case basis.

Al,

2.26.3 MCM3 and CPX Revision Requirements

It has been found that the standard CPX, p/n 2201 or 4201, must be at rev M before installing 128MB or 256MB MCM3's in a standard C2 system. If this is done it will result in à "cpx hard error". No problem exists with boards smaller than 128 MB.

In addition, it should be pointed out that MCM3's cannot be installed in C201's or C202's, as they have 1213 memories installed because of timing considerations.

.....continued on next page.....

These should be added to the tech bulletin sent out on the MCM3 under prerequisites.
Al,

2.26.4 Hardware Dump or Crash Dump

There are many situations where the crashdump is not the best way to go after a system failure. In the case of hard errors and system hangs, the hwdump utility can provide information far more quickly and with less down time for the customer.

The hwdump can be analyzed on line immediately, while the crashdump must be mailed to another office. In addition the crashdump will be unusable a great deal of the time, while the hwdump, if proper procedures are followed, is almost 100% usable. Because of limited system and personnel resources, the crashdump will not be analyzed immediately and by using hwdump this problem can be overcome by reducing the number of crash dumps to be analyzed.

The hwdump can be utilized in every situation except for a Fatal Convex Unix error. This is because the system has entered an exception handler which continues to advance the heads for sometime and by the time of the crash, the only data in the registers is from the exception handler.

The hwdump will give a great deal of insight into the problem and in many cases help determine if a crashdump will be necessary for continued troubleshooting.

In cases where a system is experiencing intermittent problems, the best troubleshooting technique is an interactive Iscan session with the hwdump as a backup. This would be performed directly after a crash and in most cases can lead to a solution after one session.

For more elusive problems a block of time should be set aside with the customer, to run PETS and perform an interactive session after any crashes during this time. This block of time should be no less than 8 hours and a request for 24 hours would be best.

By following these simple suggestions it may be possible to greatly reduce the time taken to restore the customer's system to working order. If this is explained to the customer, it will be far easier to obtain the necessary time for troubleshooting efforts.

Al,

2.26.5 FMI 81 and 82 Cautions

The FMI's 81 and 82 are required to be performed on the P1 side of the backplane. There has been a recent rash of attempts to install the FMI on the P2 side. This will not work and will result in a memory address fault when attempting to mminit. The actual fault will be an IPP 300 error and will indicate an odd data pattern of ffff7fff which indicates a problem on memory odd bit 15.

As P1 is on the bottom side of the backplane, the FE will have to be in a crouched or seated position to perform the work. If the FE is in a standing position, the FMI is being performed on the P2 side of the backplane.

Please insure that the work is being performed on the proper side of the backplane, as removal of pins and insulation can be quite time consuming and result in other problems.

Again P1 is the lower half of the backplane.

P2

EFU IPP ASP

....
....
....
....
. . .
. . .
. . .
....
....

.....continued on next page.....

P1 *

EFU IPP ASP
....
....
....
....
. . .
. . .
. . .
....
....

* P1 side is the proper side to perform FMI 81/82.

Al,

2.26.6 C2 power Calculations

Tables 1-3 and 1-5, in the Site Prep Guide, indicates a Max Phase Current for certain Processor configurations. This entry does not actually refer to a maximum achieved on a single phase, but indicates maximum current for the system.

If a maximum current for a single phase is required then the total in this category must be multiplied by .707. This will give the current for a single phase.

This total current value can be used for formulas involving KVA and Kilowatts. The Kilowatt value for a C240 should never exceed 22KW. And if it should, then this would indicate a mistake in the formula.

Al,

2.26.7 Setting SPU Time Zone

As all new systems are sent from Dallas set up for CST. It is often necessary to change this parameter in the field.

In order to accomplish this it will be necessary to determine the number of minutes the site is from GMT. For instance the central time zone is 360 minutes from GMT. In many cases this will be a negative number, as in the case of much of Europe.

The 360 minute value actually exists in the tunables file on the SPU, which is located in /mnt/os. To change this value an entry must be made in the /mnt/os/bootcmd, or bootcmd.local file. The entry would appear as the example below:

```
#Default UNIX boot command file
#
syspathname          vmunix
caches               default
root on              du0a
miniroot on          du0b
swap on              du0b

# Default to boot multi-user
howtoboot            multi_user,autoboot

# tunables...
# tune cpu number_ptys          = 32
tune cpu time_zone              = 300
tune cpu dst_algorithm          = 1
tune cpu number_tty_controllers = 4
```

As can be seen from the example above, the entry "tune cpu time_zone" is used to change this for the OS. The entry above, which is 300, would indicate Easter Standard Time.
In order to change the SPU time zone, it is only necessary to make a single entry in the /etc/time-zone file. The default would be cst, for the west coast, it would become pst, for Japan it would be JST and so on.
This should enable the time zone to be changed for each site.

Al,

2.26.8 spu4000 Failures with TLI Installed

It has been discovered that for systems with TLI installed and running 4.0, or 4.1 of system diagnostics, spu4000 will fail the CCU Scan Integrity tests. These subtests are 4400-4415.

This does not affect diagnostic release 3.5 and is what most systems with TLI installed in the field are running.

This problem will be corrected in diagnostic release 4.2.

Al,

2.27.1 spu 4000 failures with a TLI and 4.0 or 4.1 system diagnostics

It has been discovered that for systems with TLI installed and running 4.0, or 4.1 of system diagnostics, spu4000 will fail the CCU Scan Integrity tests. These subtests are 4400-4415.

This does not affect diagnostic release 3.5 and is what most systems with TLI installed in the field are running.

This problem will be corrected in diagnostic release 4.2.

Al,

2.28.1 Backplane Upgrades

It is important to understand that when performing a backplane upgrade, it is imperative that the grounds designated in the FMI be used. All vias on the right side of the slots are not grounds. In many cases they are signal vias and the use of these for a ground can result in a very dead head.

When a ground is designated in an FMI, it is selected after some investigation. If it is discovered later that for some reason a particular via does not work, it is highly recommended that the FE call the TAC to obtain another ground to use, rather than randomly choosing another one.

The results of selecting an improper via will be an extended outage and loss of confidence for the customer.

Al,

2.28.2 Adding Additional Mag Tape Controllers and Drives

The system OS is set up so that it will only recognize up to 8 mag tape units on two controllers. The following are instructions for adding additional drives and controllers:

The problem is that there is a set of structures that is statically allocated in the jp-side tape driver. When adding more tape drives than is default (8 drives or 9 for OS 9.0), you must first edit /sys/sysgen/REL_* and add the number of desired tape drives and controllers, then re-compile the /sys/dev_ccu/cpu_ta.c file.

This file cpu_ta.c has entries for all recognized subsystems. It is a simple matter to add additional MTC controllers and Tape drives in this file. The entries are the same as in the ioconfig file at the SPU. The tape entries are approximately half way down the file.

After making the proper entries in this file, it is necessary to rebuild the REL file. This can be accomplished as follows:

.....continued on next page.....

1) cd /sys/REL_*
2) make SYSTEMNAME=REL_* cpu_ta.o
3) cp cpu_ta.o ../CPU_OBJ
4) cd ../CPU_OBJ
5) cp libunix.a libunix.a.old
6) ar r libunix.a cpu_ta.o
7) ranlib libunix.a
8) cd ../REL_*
9) make install SYSTEMNAME=REL_*

This should produce a vmunix in the /sys/REL_* directory that will handle the additional tape drives. Then all that needs to happen is to copy that vmunix down to /mnt/os and / on the SPU (making backups first of course), and reboot.

Al,

2.28.3 IDCFMT Utility Information

The utility IDCFMT defaults to decimal entry for slipping and unslipping sectors. It is possible, however, to make entries in hexadecimal format as the location is displayed in error messages. This can be done in either of two options:

1) Precede the head, sector and cylinder values with a 0x. This will be recognized as hex input by IDCFMT. For example: idcfmt -d 0 0 0 slip 0x1bd 0x010 0x021

2) The other method is to precede as follows:

   a) Enter the command as idcfmt -d CCU# PORT# DRIVE# This will then respond with a prompt "idcfmt:"

   b) From the prompt an "h" can be entered to find all options.

   c) Enter "DEBUG" d) Enter base 16 e) This will change the base to hex and now a slip command can be run from the prompt. When this is exited, idcfmt will return to decimal.

Al,

2.29.1 Mag Tape Error Messages

There have been several instances in the recent past when a misleading error message from tar, "tar: Write error : EOT seen" has caused problems in diagnosing a mag tape problem. tar prints the same error message for any fatal write error. A similar error message is printed for fatal read errors.

The key to recognizing this as a misleading error message is the mux3 status bytes. In the case of the incorrect error you will not see the EOT bit set in the mux3 status bits. In addition, the mux2 status normally contains a 0x00f which indicates noise was detected during an ERASE command. The erase command is normally used in error recovery during a write operation.

The fact that no error messages are placed in the errorlog from other tape operations can also be misleading. Recoverable tape errors are not logged to the system errlog, so you may not be aware that other tape operations are experiencing tape errors.

In all instances that I have worked with, a thorough cleaning and alignment of the tape unit has corrected the problem.

Regards Dave Muir

2.29.2 C2XX HSP and Power Supply Change

For HSP's to be installed in C2's, a multi volt power supply upgrade is required. This is because the HSP/HIA combination draws more current from -5 VDC than the standard I/O subsystem draws.

The upgrade consists of replacing the -5 VDC supply with a -12 VDC supply and adjusting it to -5VDC. This provides the necessary additional current.

There is a kit provided for this upgrade, which includes the power supply and the necessary wire harness. This wire harness will add a parallel set of wires for the -5 VDC to handle the additional current load. This harness will be required for any C2 above serial number 8420. Above this, the additional wiring is standard and will only require the power supply. To verify if this harness is necessary, check the -5 VDC post at location U80 in the lower left corner of the backplane. If 2 orange wires are not run to this point, then wire harness will be required.

The part number for this kit is 550-000239-299 and the part number for the wire harness is 603-160004-200.

.....continued on next page.....

In addition the ioconfig entries for HSP are as follow:

```
hsp #
  drvr HEC-001 csr 0x00
  chnl 0-15
  type HED-001
```

A problem exists with the hsp adapter cable between the backplane and the cable to the HIA (p/n 601-600012-200). The problem is that the cable is not trimmed close enough at the connector. The symptoms are failure of class 2 subtests of dev4120, particularly subtest 241.

The solution is to trim the cable.

This is the only know diagnostic failure for the HSP.

Almost all HSP failures have been found to be cable related. So this should always be the first thought when troubleshooting in this subsystem. For diagnostic failures at subtest 4200 and above, the 3 HSP/HIA cables are nearly always the problem.

Al,

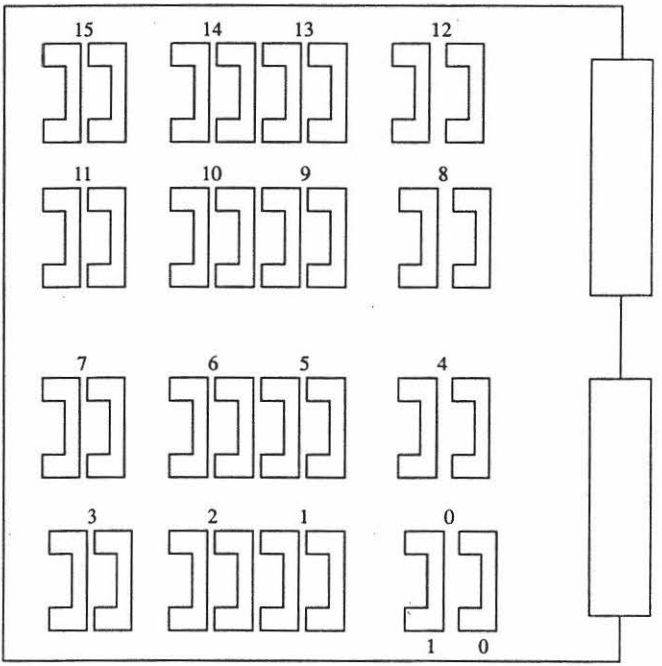
2.29.3 MCM3 Updated Information

The MCM3 is finally released and the first 2GB memory system shipped on 17 May 91. This document is intended to detail all necessary technical information concerning the MCM3. This document has been updated and replaces previous technical bulletins in week 18 and 22.
The MCM3 offers CONVEX a less expensive memory board and the capability to install up to 2GB of physical memory in all C2 products. There is no performance enhancement with the MCM3.

Like the MCM and MCM2, the failed component location can be determined from the memory address. The same basic rules apply, but is somewhat more complex because of the concept of physical and logical banks. To understand this concept, keep in mind that there are 16 physical banks on the MCM3 and it takes 2 physical banks to make up one (1) logical bank. This can be seen from the drawing and table below:

.....continued on next page.....

MCM3 PHYSICAL BANK LOCATIONS
(Each bank consists of 1 pair of DMM's)



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LOGICAL BANK	CORRESPONDING PHYSICAL BANKS
0	0,8
1	1,9
2	2,10
3	3,11
4	4,12
5	5,13
6	6,14
7	7,15

As can be seen from the table and drawing above, the physical banks that produce the actual logical bank reside on different halves of the MCM3. For example; Logical Bank is made up from physical bank 0 which is in the lower right corner of the MCM3 and physical bank 8 which is the same position on the top half of the board. It should be noticed that there are two DMM slots for each physical bank.

One other concept that is different is the fact that the MCM3 can be 1/4 or 1/2 populated. In other words you can place 8 or 16 DMM's on the board, rather than the 32 for a fully populated MCM3. To accomplish this for 1/4 populated, it is necessary to install one (1) DMM in each physical bank 0-7. In addition it is important to know that that the first DMM slot is on the right, as shown in the drawing above. Note that physical bank 0 has DMM slots labeled 0 and 1.

To produce a 1/2 populated board the same rules would apply, except that one DMM would be placed at location 0 and 1 in the lower 8 physical banks.

Because the board has so many configurations the addressing is more complex than in the past. Because of this complexity, it will be necessary to give several variations on this representation.

1Mb (256kx4) DRAMS
1/4 Populated

MCM Pairs	Physical Memory	Pair Select	Row Select	Logical Bank	Even=0 Odd =1
1	32MB	-	28	5..3	2
2	64MB	6	28	5..3	2
4	128MB	7,6	28	5..3	2

.....continued on next page.....

1/2 Populated

1	64MB	-	25,24	5..3	2
2	128MB	6	25,24	5..3	2
4	256MB	7,6	25,24	5..3	2

Fully Populated

1	128MB	-	24,25,28	5..3	2
2	256MB	6	24,25,28	5..3	2
4	512MB	7,6	24,25,28	5..3	2

4MB (1Mx4) DRAMS
1/4 Populated

1	128MB	-	28	5..3	2
2	256MB	6	28	5..3	2
4	512MB	7,6	28	5..3	2

1/2 Populated

1	256MB	-	26,28	5..3	2 **
2	512MB	6	26,28	5..3	2 **
4	1GB	7,6	26,28	5..3	2 **

Fully Populated

1	512MB	-	27,26,28	5..3	2
2	1GB	6	27,26,28	5..3	2
4	2GB	7,6	27,26,28	5..3	2

**For 1/2 populated with 8MB DMM's bit 26 is used for row select, but if used in conjunction with MCM 2's then bit 31 is used instead of 26.

Pair Select - Board Pair experiencing problem
Row Select - Indicates binary weight of DMM location
Logical Bank- Binary weight of logical bank 0-7
Even/Odd - Indicates Even or odd board in pair

.....continued on next page.....

To figure the location of the failed DMM think of the logical bank in terms of both physical banks combined. This produces DMM locations 0-3 with 2 and 3 residing in the upper physical bank. Note Drawing above for numbering of DMM locations in physical bank 0 and 8. (continues)

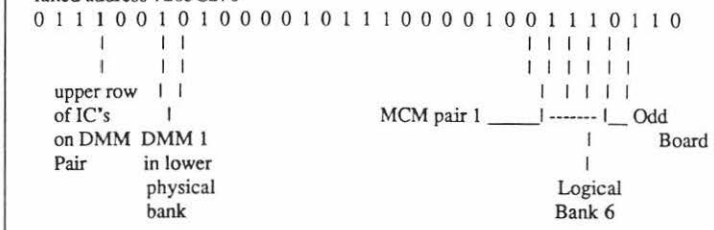
In the case of the 1/4 populated board, bit 28 just indicates the side of the DMM in error, where a 1 indicates the upper side. Keep in mind that each DMM consists of 10 DRAMs on both sides and each side is considered a row.

For the 1/2 populated board bit 24 will indicate whether the Failed part is in upper or lower physical bank and bit 25 indicates the side. For the 4MB DRAMS 28 and 26, respectively, are used for the same reference.

For fully populated boards with 1MB DRAMs bits 24 and 25 will give the location of the DMM and bit 28 will be the failed DMM row. For the 4 MB DRAMs it'll be bits 26 and 27 for the DMM slot and 28 for the DMM row.

The following example may clarify the explanation:

The example is for a system with 4 board pairs of fully populated MCM3's with 1MB DRAMs installed:



PART NUMBER

Unpopulated MCM3	410-002230-200
2MB DMM	411-000204-200
8MB DMM	411-001204-200

* 4MB DMM will only be manufactured if absolutely necessary.

.....continued on next page.....

PREREQUISITES

1) 4.1 Diagnostics
2) 4.0 Diagnostic Database
3) Diagnostic: mem4100
4) CUO 6221 and CUE 6222 for 2GB system
5) CUO 3221 and CUE 3222 for 1GB system
6) CPX 6201 for 1GB, or 2GB standard C2 system
7) PI2
   a) 1224 rev E
   b) 2224 rev H
   c) 3224 any rev
8) CPX 2201 and 4201 must be rev M when installing 128MB or 256MB MCM3's.
9) MCM3's cannot be installed in C201's or C202's, because of timing.

The MCM3 can co-exist in the same system as either the 3213 MCM, or the MCM2. It cannot, however, be installed with the 1213 MCM's.

The documentation for the MCM3 will be chapter 4 of the C3400 "Theory of Operation" Manual.

The iscan utilities mcm_func and mcm_scr have been modified for use with the MCM3.

Al,

2.29.4 DAT Tape Problem

A potential problem has been identified in some systems that are equipped with DAT tape drives. It appears that the drives may be double terminated.

The normal method of drive termination is through a SCSI cable clip-on terminator, with all the internal drive termination removed. In shipments over the past few months the drive termination has not been removed. To correct this problem all sites with DAT drives installed should be checked and the drive terminators removed. The location of the drive internal terminators is well documented in the CONVEX Digital Audio Tape Drive Service Guide (DHW-058) on page 2-12.

No known DAT failures have so far been identified as being caused by this double termination, but the problem should be correct as soon as the local conditions allow.

Kelvyn Gipp

2.30.1 IDC Crashdump Solution

As reported in this publication on week 26, the IDC and TLI have created difficulties with crashdump. A race condition has been located and the IDC has been fixed. The fix for this problem will occur on rev S boards.

A rev S IDC should be installed on any system encountering this problem. As all IDC's do not exhibit this problem, the upgrade will be performed on a failure basis only.

Al,

2.30.2 DAT Tape Quality

Only tapes that specify that they are of "Digital Grade" quality can be used in DAT tape drives. Currently only three manufacturers are known to be producing tape of this quality, and they are Memorex, Graham, and Sony. Tapes of any other quality may not produce the desired level of perfomance.

Kelvyn Gipp

2.30.3 SMD Mounting Hardware

SMD Sabre 5 disk drives are appearing in the field and can have two distinct forms of mounting hardware. The first comes in the form of a 19" rack-mount tray that can hold one, or two Sabre drives, side-by- side. The second will alow a single Sabre drive to be mounted into an NEC disk tray, adjacent to an NEC drive.

It should be understood that these two kits are NOT interchangeable.

If you are aware of installation in the future it is advisable to review the site needs for hardware and order the proper parts.

The following are part numbers for the install kits.

IPI Tray, Dual	550-000306-299	For use with two drives
IPI Tray, Single	550-000306-298	For single drive with blank panel
Sabre5 SMD Single	550-000357-200	For Sabre5 to be mounted in NEC tray.

Kelvyn Gipp

2.30.4 IOP/MIOP Mbus Pin Designations

What follows are pin designations for the MIOP and IOP.

DATA and ADDRESS SIDE

all even pins 2-60	CONGND
1 and 3	IO-MB.ADDR<13..12>
5,7,9,11,13,15,17, 19,21,23,25,27	IO-MB.ADDR<11..0>
29,31	IO.MB.DATA<15..14>
33,35,37,39,41,43, 45,47,49,51,53,55, 57,59	IO.MB.DATA<13..0>

ADDRESS and CONTROL

all odd pins 1-59	CONGND
2	IO.MB.CLK
4	IO.MB.RESET
6	MB.IO.LOCBSY
8	IO.MB.KICK
10	IO.MB.STB
12	IO.MB.MEMWR
14	IO.MB.MEMRD
16	IO.MB.BHEN
18	IO.MB.XACK
20	IO.MB.BUSY
22	IO.MB.INTAK
24	MB.IO.REQ<0>
26	MB.IO.REQ<1>
28,30	MB.IO.LOINT<0 1>
32,34	MB.IO.HIINT<0 1>
36,38	MB.IO.GRNT<0 1>
40	MB.IO.ERR
42	IO.MB.ADDRPAR
44,46	IO.MB.DATAPAR<0 1>
48	IO.MB.SEL
50,52,54,56,58,60	IO.MB.ADDR<19..14>

Al,

2.31.1 IDC Crashdump Solution

As reported in this publication on week 26, the IDC and TLI have created difficulties with crash-dump. A race condition has been located and the TLI has now been fixed. The fix for this problem will be accomplished on rev F boards.

A rev F TLI and rev S IDC should be installed on any system encountering this problem.

As all TLI/IDC's do not exhibit this problem, the upgrade will be performed on a failure basis only.

Al,

2.31.2 Interphase firmware for C1's

It has been found that the 2 byte data corruption problem, which was previously only seen on C2's, can also be experienced on C1's with Sabre5 disks installed.

FMI 80 was previously released for the Interphase VME disk controllers. This can now be expanded to include C1's as well as C2's. If it is anticipated that Sabre5 VME disks are to be installed on a C1, it is recommended that this FMI be ordered.

Our thanks to Jeff Venters, for calling this to our attention.

Al,

2.31.3 TLI Diagnostic failures

We are currently experiencing 2 TLI diagnostic failures that everyone should know about. The first is only an inconvenience and will not cause the Diag to abort. The symptom of this failure involves the following message:

```
0x1C  Try to open
Default symbols not available
```

This message can be eliminated by adding a 0 length file:

```
/mnt/test/names.idc4000
```

.....continued on next page.....

The second diagnostic problem is more severe and manifests itself as an abort of the diagnostics for all class subtests above 0. Class 0 subtests will run normally, but all other classes, beginning at subtest 1010 will abort under dshell and when attempting to run tli4480.t at the spu prompt the error "IOT trap; Core dump" will be encountered.

This problem can be quickly solved with the insertion of a rev K SP4. All revs below K will cause this failure.
Al,

2.31.4 Common error troubleshooting

I have sent this out previously, but I'm sending it again for those that have misplaced or did not receive the first transmission.

Below are some very basic tips for troubleshooting the most common errors on C2's. This is not intended as an indepth discussion on these errors, but only to point the FE in the right direction. This does not include all errors, but for now, only the most common. This list is compiled as a result of solutions on actual systems in the field. The percentages reflect the number of systems fixed with the various options.

1) IPP 300 error - This crash is an mbus parity error (memory). This crash can be found by the use of the mbus utility. Generally the error will be found in the memory crossbar or the DFW gate array on the ASP. Recommended suspects:
   a) memory 50% (MCM replaced that contains parity error)
   b) ASP 40% (Found by location of error)
   c) IPP 10%

2) ASP 101 - This problem can be pursued with the mbus utility as well. Generally the error will show in the DFW gate array or the register file.
   a) ASP 70%
   b) VPD 30%

3) PI 653 - This problem can be located by using PI2_func. Quite often memory address is displayed as the ebus_addr on the ebus screen. If the error is not found in memory then the fault is the PI2.
   a) MCM 65%
   b) PI2 35%

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4)PIA 602 - Very similar to the 653 above, but only occurs on C2's with PIA's. This error is an ebus read error and is generally considered memory related. The error generally includes a memory address. When it doesn't the problem can often be found with cpu4041.

a) MCM 90%
b) PIA 10%

5) VPD 804 - This error can almost always be found with cpu4241 and a VL of 16.

a) VPD 90%
b) other 10%

6) IOconfigure -1 - This error, although indicating IO, is most often found in a defective CPU. The error can be an incompatible IO module (IOP, VIOP) under /mnt/os at the spu. The software should be considered if the problem happens after an OS upgrade. Usually cpu4041 and cpu4241 is helpful in isolating the cause. A full hwdump can also be helpful. This error can be confirmed as CPU by simply moving a new controller to the top of ioconfig file. As during the boot sequence, each head performs the same functions, it may be helpful to disable a head and boot.

a) ASP 30%
b) VPD 30%
c) IPP 10%
d) MCM 10%
e) foreplane 10%
f) OS 10%

7) ASP 104 - This error could be caused by, literally, anything. Quite often this error will accompany other problems and only serve to cloud the issue. If this error accompanies other crashes then generally this problem will be corrected when the other is solved. If this error occurs by itself, it will only be beaten by a very thorough analysis, involving Iscn and crashdump. Generally hwdump will be of little use, but a thorough interactive scan can help.

8) MCM 501 - Is always memory related. This problem can almost always solved with the use of the mcm_scr utility, or mcm_func. The diag cpu4041 can also be helpful in pursuing this problem.

9) CUE 483 - This problem indicates a vector control store parity error. No action should be taken on the first occurrance because noise or other random interference can cause them. But, if more than one crash occurs this problem is always a VPC.

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10) Cache Controller Error - Always indicates a bus (mbus or VME) failure. This error almost always indicates a defective controller, but locks the bus and prevents a useful error. The only useful procedure is to distribute controllers on this bus to other IO busses, thus isolating the failure. Warning: Do not fall for error messages as these will refer to last successful transfer.

11) Cable error - Indicates individual controller failure, but associated information is usable and will generally lead to failing component. This error will generally not cause a system crash.

12) kern trap - Generally indicates an IO bus related problem, but can indicate a CCU or PIA failure. Accompanying error printout is very useful in pursuing this symptom.
    a) IO controller 60%
    b) CCU 20%
    c) PIA 20%

Al,

2.32.1 Revised mcm_func for MCM3

With the introduction of the MCM3, it was necessary to modify the Iscan utility mcm_func. This was necessary to cover the differences in board layout and the introduction of Javelin. This article will cover the differences in mcm_func between MCM's and MCM3's. All switches will work the same for MCM's, but when scanning a MCM3, there will be major differences.

For additional information, refer to Scan-003 tech tip on mcm_func and the most recent Tech Bulletin article on MCM3. Between all 3 articles, everything should be explained.

AL,

---

dump_win_q <mcm slot #> -- For MCM1s and MCM2s this function dumps the Win Queue which contains info on the last 16 accesses to memory. This queue is only for diagnostic purposes. When new items are pushed into the queue the address is incremented. There is an example of this dump plus a description of each field towards the end of this document. The MCM slot numbers for C2xx systems are labeled 0,1,2,3,4,5,6,7 which are for MCM even0, odd0, even1, odd1, even2, odd2, even3, odd3.

For MCM3s this function basically does the same thing as it does for MCM1s and MCM2s the differences being that the MCM3's win queue contains more info. This function dumps the 16 most recent Win queue entries of its 256 entries. When new items are pushed into the queue the address is incremented. On the MCM3 the win queue is in the log ring, any soft error will lock up the log scan ring. There is an example of this dump plus a description of each field towards the end of this document. The MCM slot numbers for Javelin systems are labeled MCM slots 0,2,4,6,1,3,5,7 which are for MCM even0, even1, even2, even3, odd0, odd1, odd2 and odd3.

dump_rd_q <port>,<mcm slot #> -- Dump the contents of XBAR read queue. This queue is 8 deep which contains read data from memory. This function works on all MCM types and the format of the display is the same. An example of a read queue dump plus a description of each field is located towards the end of this document. This function works with all mcm types.

xbar_ptr <port>,<mcm slot #> -- Dump the read and write pointers of all the XBAR gate arrays for the specified port and MCM. This function works with all MCM types.

mcm_err -- A scan function that determines if there are any hard errors or soft errors present on any of the installed MCM1s or MCM3s in the system. This script will not work with MCM2s If errors are found it will display MCM slot number and pertinent info about the error, if no errors are found nothing is displayed.

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howto -- When executed this procedure will display on the screen the use and short description of all the scan scripts in this file "mcm_func".

dump_win_q example:

```
-- current register contents for MCM[4] --
win_q_adr     qpx_win     qm_start      rpx_win     rm_start
    0             7           0             4           1

-- contents of the win queue for MCM[4] --
     adr      win     start
      f        4       80
      e        4       40
      d        4       20
      c        4       10
      b        0        8
      a        0        4
      9        0        2
      8        4        1
      7        4       80
      6        4       40
      5        4       20
      4        4       10
      3        4        8
      2        4        4
      1        4        2
      0        4        1
```

Most recent memory request info at the top of display, least recent at the bottom of the display.

win_q_adr -- The address of the win queue, this is a four bit field. The address is post incremented (bumped after access) value of the win address.

qpx_win -- A 7 if idle, nothing getting pushed into the queue. If not a 7 then a push is active and the number is equal to the port making the request; i.e. 0 = Port A, 4 = Port E ...etc.

qm_start -- If a push into the queue is active then this will indicate which bank the request is for. If a push is not active then this field will be a zero. An 8 bit field (displayed in hex), only one bit set at a time, where bits 7-0 corresponds to banks 7-0.

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rpx_win -- The contents of a register that is being driven by the output of the Win queue. The info is from where the post incremented Win address is pointing to. Indicates which port that item was for, 0-4. Usually a piece of useless info.

rm_start -- The bank info from the item the Win queue adr is pointing. Usually a piece of useless info.

adr -- The address into the Win queue. The top item is the most recent access to memory. The bottom item the least recent.

win -- Which port the access to memory is for, 0 - 4. 0 = Port A; 4 = Port E ...etc.

start -- Which bank the request was for. An 8 bit field, one bit for each bank, displayed in hex. Where bit 7 - 0 corresponds to bank 7 - 0. Looking at the top item of the example the start field is 80 which indicates this request was for bank 7, the next item down was made for bank 6.

dump_win_q example for MCM3

```
     -- contents of the win queue for MCM[0] --

scan config = 1
winq_addr   win   start<7..0>     addr  row_sel   owner   bkpl_addr
   a1         0      0000 0010     0eeb9       5       0    113b2e48
   a0         1      0010 0000     e79ef       2       0    029efbe8
   9f         0      0000 0001     0eeb9       5       0    113b2e40
   9e         1      0001 0000     e79ef       2       0    029efbe0
   9d         0      1000 0000     2e6b9       5       0    11b92e78
   9c         1      0000 1000     e79ef       2       0    029efbd8
   9b         0      0100 0000     2e6b9       5       0    11b92e70
   9a         1      0000 0100     e79ef       2       0    029efbd0
   99         0      0010 0000     2e6b9       5       0    11b92e68
   98         1      0000 0010     e79ef       2       0    029efbc8
   97         0      0001 0000     2e6b9       5       0    11b92e60
```

Most recent memory request info at the top of display, least recent at the bottom of the display.

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scan_config -- A 2 bit field which determines which addresses are used for the row_selects.

Scan Config Register	Row Select		
<1..0>	<2>	<1>	<0>
0 0	27	25	24
0 1	24	25	28
1 0	27	31	28
1 1	27	26	28

winq_addr -- The address of the win queue, this is a eight bit field. The win queue address equals zero after reset and is incremented after a entry has been made.

win -- A three bit field which will indicate which port an entry is for; i.e. 0 = Port A, 1 = Port B,..., 4 = Port E. A seven (7) in this field would indicate that the entry is not valid. You should never see a 5 or 6 in this field since they are not used.

start<7..0> -- If the queue entry is valid then this will indicate which logical memory bank the request is for. This is an eight bit field (displayed in binary), only one bit should be set at a time. The bit that is set indicates which logical bank the request is for, where bits <7..0> correspond to logical banks <7..0>. Note the actual scan fields read for this information are active low, I am inverting them in the script to make it easier to read.

addr -- This is a copy of the address which is used to access the rams with.

row_sel -- A three bit field which determines which row and physical bank of memory the request is for. Bit two being set to a one (1) indicates that the request is for the upper physical bank of the physical pair. An example of this is that if there is a start for logical bank 0 and row_sel<2> equals a 1 then the request is for physical bank 8. If row_sel<2> is a zero (0) instead then the request would be for physical bank zero (0). Below is a table showing the logical banks and the corresponding physical banks.

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Logical Bank	Corresponding Phys. Banks
0	0, 8
1	1, 9
2	2, 10
3	3, 11
4	4, 12
5	5, 13
6	6, 14
7	7, 15

owner -- If the win queue entry is for one of the CPU ports; i.e. 0-3; this field in conjunction with the "WIN" field will enable you to determine which CPU owned the memory port for a paticular request. This is only valid when the MCM3 is used in a Javelin. The table below should explain how to interpret the WIN & Owner fields.

WIN	Req_ Owner	Requesting CPU	Memory Port Used
0	0	CPU 1	A
0	1	CPU 0	A
1	0	CPU 3	B
1	1	CPU 2	B
2	0	CPU 5	C
2	1	CPU 4	C
3	0	CPU 7	D
3	1	CPU 6	D
4	X	NONE	E

bkpl_addr -- This is the actual address sent to the MCM3 from the board making the memory request. This is not actually part of the win queue but is derived from the info provided by the win queue entries. This was added to this script to help in debug efforts.

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dump_rd_q

```
iscn==>dump_rd_q 0,0       "Iscn Command"
-- XBAR read queue contents for port A of MCM[0] --
rd_ptr     wr_ptr     rd_par     rd_dat
  40          8          f       ffffffff (Current)
  40          8          f       ffffffff (after 1 clock)
  20          8          e       1b840054
  10          8          d       537503
   8          8          9       50515253
   4          8          9       50515253
   2          8          4       73ffd01f
   1          8          4       73ffd01f
  80          8          f       ffffffff
```

One thing to note about the display of this function is the comments (current) and (after one clock). When the function is executed it saves off the top item of the Read data queue then gives the MCM one more clock, and prints out the whole queue. If the wr_ptr (write pointer) has changed from the "current" and "after 1 clock" line then a push of the queue just happened.

rd_ptr -- The read pointer for the read data queue, located in the Xbar gate arrays. The top of the queue is displayed at the top of the screen, the next item to be popped if the queue is not empty. Item popped if a Read Enable is received from the requesting port. This pointer is 8 bits, starts at 01 and counts 01, 02, 04, 08, 10, ...etc.
wr_ptr -- The write pointer for the Read Data Queue, pointing at where the next item is to be pushed into the queue. Item being, read data returning from the ECC gate arrays. This is a four bit field that counts from 1, 3, 7, F, E, C, 8, 0, tentatively known as a Gaynel Counter.

rd_par -- The read data parity bits, part of the data that is pushed into the queue. Odd parity, MS-parity bit for MS-data byte.

rd_dat -- Read data that is pushed into the queue.

rcnt -- Counts up when a read memory request is taken by the MCM. Counts down when the MCM gets a Read Enable.

dcnt -- Counts up when the ECC gate arrays returns data to the XBARS, and counts down when the MCM receives a Read Enable from requesting ports. If rcnt and dcnt are equal then the ECC has returned all requested read data back to the XBAR.

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**Note: There is a bug found that if a RD_ACK is asserted at the time this script is executed, the rd_ptr will change between the current and after one clock line.

xbar_ptr

```
iscn==>xbar_ptr 0,0       "Iscn Command"
-- XBAR rd/wr pointers for port A of MCM[0] --
rd_ptr:   xbar0  xbar1  xbar2  xbar3  xbar4  xbar5  xbar6  xbar7
            80     80     80     80     80     80     80     80

wr_ptr:   xbar0  xbar1  xbar2  xbar3  xbar4  xbar5  xbar6  xbar7
             0      0      0      0      0      0      0      0
```

This script was written to make it easier in determining which XBAR is the culprit if the MCM has unequal rd or wr pointers. The rd/wr pointers should always be equal under normal operations. The screen "port" in "mcm_scr" will indicate if a given MCM has unequal read or write pointers, see the info on mcm_scr for more detail.

mcm_err Examples

There are several variations of formats which are displayed with the "mcm_err" script. The type of display is dependent on the type of error and whether the board is a MCM1 or MCM3. This script will not work with MCM2s. Below will be explanations of all the various display formats.

```
mcm_err (MCM1 hard error)

MCM1 Hard error reported by MCM[7]
Bank 5 detected a parity error
Write Parity = 0
Write Data = 0
1 parity error (s) found on MCM[7]:
0 multi-bit ecc error (s) found on MCM[7]:
0 single-bit ecc error (s) found on MCM[7]:
```

This format is displayed for MCM1s when only a write parity error is detected. The first part of this display informs you of which board pulled the hard error. The next line informs you of the bank that detected the write data parity error.

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Write Parity -- The parity for the data that caused the write data parity error. The ECC gate array uses odd parity where the ms-parity bit is for the msb of data and the ls-parity bit is for the lsb of data. Note that write parity is checked when there is a valid memory request, whether the request is for a write or not. (continues)

Write Data -- This is the data read from memory on which the parity error was detected.

The last three lines of this display informs you of how many different types of errors was found on this one MCM1.

```
mcm_err (MCM1 multi-bit)
MCM1 Hard error reported by MCM[7}
Bank 4 detected a multi-bit ecc error
    Read Data      = 5a5a991f
    Read ECC       = 5a
    Generated ECC = 58
0 parity error (s) found on MCM[7]:
1 multi-bit ecc error (s) found on MCM[7]:
0 single-bit ecc error (s) found on MCM[7]:
```

The first line of the display informs you of which MCM1 has a hard error. The second line of the display indicates which bank a multi-bit ECC was detected on.

Read Data -- This is the data read from memory which has a multi-bit ECC error.

Read ECC -- This is the ECC read from memory for the data with a multi-bit ecc error.

Generated ECC -- This is the ECC generated for the data read from memory. The generated ECC is compared to the ECC that is stored in memory with the data.

The last three lines of this display informs you of how many different types of errors was found on this one MCM1.

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```
mcm_err (MCM1 single-bit)

MCM1 Soft error reported by MCM[6]
Bank 3 detected a single-bit ecc error
    Read Data      = 5a5a991f
    Read ECC       = 5a
    Generated ECC = 58
0 parity error (s) found on MCM[6]:
0 multi-bit ecc error (s) found on MCM[6]:
1 single-bit ecc error (s) found on MCM[6]:
```

See the multi-bit ECC field descriptions for more details. This display is basically the same as the display for the multi-bit ECC. A single-bit ECC error is correctable so hard error is not pulled in these cases.

(mcm_err example (MCM3 harderr)

```
iscn==> mcm_err "Iscn Command"

MCM3 Hard error reported by MCM[1]
Phys. Bank 9 detected a hard error; Logical Bank 1
becc[9].harderr = 1       becc[9].softerror = 0

wr_data       = 00000000 wr_parity = 0
dd_scan       = 00000000 cb_scan   = 00
rddata_log    = 00000000 rd_ecc    = 00 gen_ecc = 31
cycle_type    = 0 No-Op
err_type_log = 0 ECC Hard Error

win = 3       req_owner = 0         row_sel = 5
ram addr = df465       bkpl addr = b7d1948
```

Note at the time this documentation was done it was still being debated whether the field err_type_log will always give you valid info, so keep this in mind.

becc[n].harderr = n becc[n].softerr = n -- These are the BECC gate array's internal error conditions. This info is only displayed for BECCs with errors. After the script has determined which board has a soft or hard error then it checks all 16 BECCs to determine which one(s) caused the board's soft/ hard error. Info is only displayed for the BECCs that have errors.

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wr_data = n wr_parity = n -- This is the write data and its parity into the BECC. If the hard error was caused by a write data parity error these fields will have the bad data and parity captured. This is even parity where the ms-parity bit is for the ms-byte of data and the ls-parity bit is for the lsb of data.

dd_scan -- This register is in the dmode ring, it contains the data bits from the rams on read or test and modify operations. This field is useful if the board's softerr and harderr bits are both set. In this case it will help you in determining if a soft error occurred before the hard error was detected. If the softerror and harderror are set then; If ((dd_scan = rddatalog) & (cb_scan = rd_ecc)) then the hard error occurred at the same time as the soft error otherwise the soft error occurred first. This will be explained in further detail at the end of these field descriptions.

cb_scan -- This register is in the dmode ring, it contains the check bits on read or test and modify operations. This field is useful if the board's softerr and harderr are both set. In this case it will help you in determining if a soft error occurred before the hard error was detected. This will be explained in further detail at the end of these field descriptions. (continues)

rddata_log -- This register is in the log ring, if the BECC detects an ecc error this register will hold the data bits that were read from memory.

rd_ecc -- This register, which is in the log ring, will hold the check bits from memory if an ecc error is detected.

gen_ecc -- This register, which is in the log ring, will hold the check bits that were generated on the data read from memory if a ecc error is detected.

cycle_type -- A two bit field in the log ring which will indicate what kind of operation the BECC was in the process of doing at the time a error is detected. In cases where there is a hard and soft error and the soft error occurred first then this field will only contain info on the soft error.

err_type_log -- A two bit field in the log ring which should indicate to you the reason the BECC pulled a hard error, unless a soft error occurred first then the info is not valid.

req_owner -- If the "win" field is for one of the CPU ports; i.e. 0-3; then this field in conjunction with the "win" field will enable you to determine which CPU owned the memory port for this request.

row_sel -- Is the row select for the memory request which caused the error. This is a three bit field which determines which row and physical bank of memory the request is for.

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ram addr / bkpl addr -- This is the memory address to the rams at the time of the failure. Keep in mind that this information is in the Log ring. The ram address is obtained from the win queue. The script is limited to searching through only the most recent 16 locations of the win queue for the failing bank. If the failing bank is not found in these 16 locations a message stating this is displayed instead of the address.

In trying to determine why a MCM3 has pulled a hard error two things you need to keep in mind. One is that when a soft error occurs it locks up the log scan ring until the SP4 clears it out. So if a soft error occurs before a hard error a lot of the info might not pertain to the cause of the hard error but for the soft error. Second thing to remember is the info in the err_type_log field might not be valid. See the table below:

MCM3 hard error conditions -- when harderr occurs first or at same time as softerr

Error cause	harderr	softerr	((DDSCAN = RDDATALOG) & (CBSCAN = CBREGLOG))	Write parity error exist
Slow Data	true	false	true	false
Write Parity	true	false	true	true
Multi-bit ECC	true	true	true	false

MCM3 hard error conditions -- when softerr occurs first

Error cause	harderr	softerr	((DDSCAN = RDDATALOG) & (CBSCAN = CBREGLOG))	Write parity error exist
Slow Data	true	true	false	false
Write Parity	true	true	false	true
Multi-bit ECC	true	true	false	false=

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```
mcm_err (MCM3 soft error)
iscn==> mcm_err              "Iscn Command"
MCM3 Soft error reported by MCM[1]
becc[1].softerror = 1
single-bit ecc error found in phys. bank 1; Log. bank 1

rddata_log = 00000000  rd_ecc = 00  gen_ecc = 31
win = 3          req_owner = 0        row_sel = 5
ram addr = df465        bkpl addr =  b7d1948
```

This format of the "mcm_err" is displayed for MCM3's when there is only a soft error present and no hard error; i.e. single bit ECC error. See the MCM3 hard error field descriptions above for field definitions.

2.32.2 IDC and TLI revision levels for C3

There are new revision levels for the IDC and TLI to allow them to function in the new C3 Neptune. This increases the rev of IDC to T and the TLI to G. These revs will be required to install these units in Neptune system. These revs are downward compatible and will also function in the current systems. This is not required for Javelin.

The purpose of the changes was to allow the CCU's to function in the extended address scheme of the new systems.

The current plan calls for shipping new CCU's with new systems and in the case of place holders, have the site personnel return the down rev CCU's for upgrade. These upgrades will be required for HSP and VIOP, as well and these changes will be released soon.

Al,

2.33.1 Loading a Virgin SPU Disk

It has been discovered that there are some inconsistencies in the procedure to reload a virgin SPU disk. These problems can be easily overcome by following this procedure for loading the SPU from scratch. This procedure is for a blank disk only and the situation does not affect currently loaded disks.

The basic problem is that Diag_db needs the cop.out file loaded before continuing. This file does not need anything in it, but the zero length file must be present.

To load the spu after format of disk:

1) Load SPU Unix
2) Boot from front panel with mode set to Diag.
3) At the spu prompt create file " /mnt/usr/scn/cop.out"
4) Load Diag_db
5) Load Diags

Al,

2.33.2 Re-booting After an ASP-104 Error

It has, recently, become apparent that it is necessary to use the master reset switch on the front panel after encountering an ASP104 failure. After a crash it appears that a standard reboot after an initall does not clean up sufficiently and in most cases the system will encounter another crash in a very short time period. In some cases, it has even been found that the error persists on the reboot effort.

The recommended recovery procedure after an ASP104 error is to take the system to front panel and exercise the master reset switch and then reboot. This will create a little more down time up front, but will increase the time between failures significantly. NOTE: This should only be done after all information has been obtained.

The ASP104 error is a microcode corruption and can be caused by almost anything, but in almost all cases, does not involve the ASP. The most common cause is an EFU out of tune. In many cases, moving this EFU to another head will result in a different failure, particularly RITA address or data parity errors. The other most likely causes of this crash are the EDC and IPP respectively.

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This crash is vastly different from other hard crashes and should be handled accordingly. A hardware dump is of little use in this case, but an interactive scan session, directly following the crash, can yield some results. This is not a direct benefit, but some of the more common signatures can be found by an experienced engineer.

The cause of these crashes can be very difficult to locate and random board swapping should be avoided, because this will generally make the situation even worse. Doing nothing on the first occurrence is preferable to random board swapping, but a thorough analysis at the time of the crash

These crashes will also occur after another, different, system crash if a proper reboot procedure is not followed after the initial crash. These ASP104's are generally a false indication and are a result of the previous crash. These errors can also accompany other crashes and because of this, the accompanying crash should always be pursued rather than the ASP104.

Al,

2.33.3 Ethernet Error Messages

The following table is a list of current ethernet error messages used since the introduction of 9.0. The general error format will appear as GET_ETHERNET_STATS number. This number can then be used to determine the actual error message. For example a 1638400 would be EX_OFFLINE which would indicate that the controller is offline.

EXOS_SELF_TEST_TIMEOUT	= 65536
EXOS_CONF_MSG_SEND_TIMEOUT	= 131072
EXOS_CONFIG_COMPLETION_TIMEOUT	= 196608
EXOS_CONFIG_FAILURE	= 262144
EXALLOC_REQUESTQ_NOSPACE	= 327680
EXALLOC_REPLYQ_NOSPACE	= 393216
EXALLOC_QH_NOSPACE	= 458752
EXALLOC_CONF_NOSPACE	= 524288
EXALLOC_NOWNDW	= 589824
EXALLOC_DBGPG_NOSPACE	= 655360
PROBE_NO_CONTROLLER	= 720896
PROBE_RESET_TIMEOUT	= 786432
PROBE_DATABASE_TOOBIG	= 851968

.....continued on next page.....

EXSEND_TIMEOUT	= 917504
EXGETSTAT_NO_WNDW	= 983040
EXCONTROL_NET_MODE	= 1048576
EXCONTROL_NET_ADDRS	= 1114112
EXCONTROL_NET_RECV	= 1179648
EXCONTROL_NET_STSTCS	= 1245184
EXCONTROL_EINVAL	= 1310720
EXRECEIVE_RECEIVE	= 1376256
EXTRANSMIT_TRANSMIT	= 1441792
EX_EINVAL	= 1507328
EX_OFFLINE	= 1638400
EX_SUCCESS_MEMCSR	= 1966080
EX_SUCCESS_IOCSR	= 2031616
EX_BOARD_RESET	= 2097152
EX_BOARD_CONFIG	= 2162688
EX_INVALID_MODE	= 2228224
EX_INVALID_MODE	= 2228224
EX_RESTART_ERROR	= 2293760
NUM_EX_TOO_BIG	= 65601536
NO_MBS_BUFS	= 65667072
CCUDEV_CONFIG_TM_SEND	= 65732608
CONFIGURE_TM_SEND	= 65798144
NO_RECEIVE_BUFS	= 65863680
NO_TRANSMIT_BUFS	= 65929216

Al,

2.34.1 Release 4.0 Diagnostic Error Message

It should be noted that when initiating tests under diagnostic releases at 4.0 and above, the following message will be printed:

"Unable to determine software revision"

This is not a major problem and only indicates that the revision stamping mechanism is defective. This message should be ignored. It has been noted and reported and will be fixed in future releases.

Al,

2.34.2 Crashdump and hwdump Problem on large C240 systems

A problem has been discovered involving very large C240's and crashdump and hwdump utilities. This problem is configuration dependent and is somewhat difficult to predict.

The problem manifests itself as a failure in the hwdump utility, or the hwdump portion of the crashdump -H. This failure is generally seen as a "Memory fault - core dump" message before the hardware dump is complete. Normally the fault will occur directly after dumping the registers and micro stack for the third head.

This problem occurs, only on 4 headed systems with 8 memory boards, particularly MCM3's, and very large I/O subsystems, usually involving multiple IDC's and/or TLI's. The problem is that the SPU memory is not large enough to accommodate the very large scan definitions and the full hwdump.

The problem has been reported and is being investigated. In the mean time there is a patch available. If this problem is noted on a system, please contact hardware support and the solution will be provided. The solution is too complex to report here and will affect so few systems as to be a waste of space here. The solution will involve editing the hwdump, hwdump_fast and hwdump_iscn files located in /hw/cputest, on the SPU.

This problem is not caused by crashdump, but is produced by the hardware dump portion of this utility. A straight crashdump will work, only the -H option will cause it to fail.

Again, this problem is very limited and will only occur on very large configurations. From this point on, Systems test has agreed to perform a crashdump -H on all systems prior to shipment.

Al,

2.34.3 Minimum Usable Revision Levels

It is recommended that all field parts be at a minimum of the below rev levels. These rev levels are downward compatible to most rev's while allowing use with the more up to date systems. These minimum rev levels will allow the most coverage for C2 systems and reduce the possibility of rev level incompatibilities. It makes little sense to continue to stock down rev'd modules that have little relevance to current configurations and in many cases will not function.

	MODULE	P/N	MIN REV	
1)	ASP	1209	M	
2)	VPC	2205	G	
3)	VPC	1205	G	
4)	DCU	1208	R	
5)	IPP	1207	K	
6)	SFU	1210	H	
7)	EFU	3220	N	* EFU 1220 and 2220 and EDC 1219's should
8)	EDC	2219	J	* be scheduled with logistics for upgrade.
9)	SP2	1200	N	
10)	SP4	1223	K	
11)	PIA	1212	M	
12)	PIA	2212	J	
13)	MPIA	3212	J	
14)	PI2	1224	E	
15)	PI2	2224	H	
16)	VPD	1206	H	
17)	CPX	2201	J	
18)	SCM	0130	X	
19)	SCM	0168	G	
20)	ESM	1180	P	
21)	IDC	1228	L	
22)	TLI	1269	D	
23)	VIOP	2149	J	

NOTE

These rev's should not be confused with the minimum shippable rev's published in the configurator's.

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For all boards that fall below these rev's, it is recommended that they be upgraded soon. As stated earlier, these minimum rev's should allow these boards to be used in the widest number of situations and also incorporate fixes that are considered mandatory.

If the module does not fall on this list then a minimum usable rev has not been determined or is not applicable. These rev's should provide the best probability of the replacement module being compatible in the affected system. This list does not solve all possible minimum rev situations, but is a solution to the vast majority of situations.

Al,

2.34.4 Mixing MCM Types

It should be noted that 1213 and 3213 MCM's cannot reside in the same system. There are timing differences between these two boards and if installed in the same system can this result in intermittent memory related failures. In addition, warnings will be generated at the SPU when trying to initall or mminit.

The minimum rev level requirements for 3213 MCM's:

1) ASP rev K
2) SP2 REV L
3) PIA REV H

Al,

2.34.5 VIOP Device Driver Memory Usage

Much has been written and said regarding VIOP memory requirements for systems, and how to determine if your particular configuration will have problems configuring or booting. Starting with the release of ConvexOS 9.1, a document titled "ConvexOS VIOP Device Driver Memory Usage" was released along with all the normal release paper- work. This document shows all currently available devices that require a device driver and how much VIOP memory each controller device driver will take. The information given in this document will allow the total system VIOP memory usage to be calculated. This document is planned to be released with every OS release and will provide revised/new VIOP memory values as they become available.

The current release of the document mentioned above is document number 710-003430-022, dated May 1991.

Kelvyn Gipp

2.34.6 TLI/STC 4480-8 Problem

STK has recently introduced an eight channel controller that connects their tape silo subsystem to a number of computer systems, one being a Convex, through our TLI controller. TLI connections to STC silos in the past have been through a four channel controller. Some sites who recently tried to connect through the new eight channel controller ran into problems while trying to run "tli4480 class 4 diagnostics. This problem has been corrected by STK and tested by Convex. If you have a site that either has or will soon be getting an STC 4480-8 CU please check to see that it contains a BC-B interface board with a P/N of 404277303. No changes are required if TLI connection will be through a four channel control unit.

Kelvyn Gipp

2.35.1 DKD-281 Disktab Entry Revisited

A Technical Bulletin was sent out by Dan Schoner in the Vol 2 week 25 release, which advised of the correct disktab entries for use with a DKD-281 Sabre5 SMD disk drive.

It should be noted that ALL current releases of ConvexOS 9.1 and 9.1.? do not have the correct disktab entries in them as was originally planned. It should also be noted that there are no plans to correct this problem until OS 10.0 is released.

Please continue to use the information provided in the Technical Bulletin that was released by Dan. While this error only affects sites using Sabre5 drives, all sites, regardless of the drives in use, should correct their disktab entries for the DKD-281 drive.

Kelvyn

2.35.2 vasync Device Status

The following information is provided to assist in understanding Vasync Device Status returned during the Vasync Printer Test, should a failure occur.

as an example: Expected: 0x09 actual 0x0b at address 0x????????

Only five (5) bits of the status are needed.

```
0x0b = 0000 1011
|  ||||
|  |||+-- SLCT
|  ||+--- RDY
|  |+---- DR
|  +----- FIFO empty ]
|  ]> These two signals are from
+------- FIFO full ] the VASYNC FIFO
```

In the example shown the diagnostic was expecting the printer to return a SLCT signal, and for the VASYNC FIFO to be empty, but it received a printer RDY signal as well, that was unexpected.

Kelvyn

2.35.3 Power Supply Requirements in C2 Series

After some testing, I've determined that if the system configuration does not require all supplies, mainly -4.5VDC, and one fails to contribute current share, the other supplies will support the load. The other supplies will then support the load and this failure will not crash the system. The only indication will be a display 0f 89, 99 on the front panel.

If this configuration is allowed to run for any period of time, then it is possible that remaining supplies will fail when the system is powered off.

Thanks to Gene Morozov for reporting his observations of a system in this state.

Al,

2.35.4 MEM4100 Diagnostic Information

Now that memory diagnostic mem4100 has officially replaced mem4000 as the standard memory verification, as of diagnostic release 4.0, it is time to give some general explanation.

Essentially mem4100 is an improvement on the basic mem4000 diag. It is far more robust and uses 4 error detection algorithms. Many of the subtests are direct ports from mem4000, but there are many more that are brand new. There are 5 classes of subtests and they are as follow:

Class 1 Arbitration and crossbar tests

Class 2 Service Processor based tests, for functionality. These are all new and run the same basic tests as class, only from the SPU side. This enhances error evaluation.

Class 3 Service Processor based tests for exception functionally. These tests are for MCM and MCM2 only.

Class 4 Same as class 3, but for MCM3 only.

Class 5 CPU based tests for memory. There are several options available with the test, that provide some additional analysis features and capability.

2: Generate PCM. A no answer will force the diag to use the pcm already created in /mnt/boot_db and not create its own. This can be useful in testing a specific configuration when it isn't necessary to test all of memory.

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3: Memory pairs to test Self explanatory. Must be one full pair.

4: Run Exhaustive subtests. A no answer will allow subtests 4200-4207 to be skipped. These tests are quite long and will dramatically increase test time, if run.

5: Use CPU(s) to test memory. The default is yes, but if no, then this will test from SPU only.

6: CPU(s) to use. This will allow the testing of specific heads. The heads to test will be specified by entering 0-3.

7: Load code at lower or upper memory. The default loads code in lower memory. An e will load the diag into upper memory and allow the lower memory to be tested.

8: Halt CPU on error. The default here is to loop on an error, but to stop clocks and halt the processor immediately, enter yes.

The only known failure is a possible failure of subtest 5120 with 3 heads. This subtest is a cpu address = data test will all heads. All other subtests should run with no failures.

Subtests are as follow:

subtest	class	description
1025	1	Arbitration win logic
1200	1	crossbar read/ write latching
2000	2	SPU zone bit functionality
2010	2	SPU scrub operations
2020	2	SPU test and set
2030	2	SPU test and clear
2100	2	SPU address = data
2200	2	SPU MATS+ data bit patterns
2210	2	SPU MATS+ alternate data bit patterns
2220	2	SPU MATS+ data and ECC patterns
2230	2	SPU MATS+ ECC patterns
2300	2	SPU data pattern algorithms
2310	2	SPU alternate data algorithms
2320	2	SPU data and ECC algorithms
2330	2	SPU ECC pattern algorithms

**NOTE All class 3 test for MCM and MCM2 only.

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3020	3	Arbitration win queue
3150	3	SCAN testing for normal ECC / parity
3151	3	SCAN testing of write parity error detection
3152	3	SCAN testing of single bit ECC detection, data bits
3153	3	SCAN testing of single bit ECC detection, check bits
3154	3	SCAN testing of double bit ECC detection, data bits
3155	3	SCAN testing of double bit ECC detection, check bits
3156	3	SCAN testing of single bit ECC detection, partial writes
3157	3	SCAN testing of single bit ECC detection, TAM
3158	3	SCAN testing of scrub operation
3160	3	EBUS testing of normal ECC / parity
3161	3	EBUS testing of read parity error detection

**NOTE All class 4 tests for MCM3 only.

4000	4	ECC, memory even zero
4001	4	ECC, memory odd zero
4002	4	ECC, memory even one
4003	4	ECC, memory odd one
4004	4	ECC, memory even two
4005	4	ECC, memory odd two
4006	4	ECC, memory even three
4007	4	ECC, memory odd three
4100	4	rd/wr parity error detection, memory even zero
4101	4	" memory odd zero
4102	4	" memory even one
4103	4	" memory odd one
4104	4	" memory even two
4105	4	" memory odd two
4106	4	" memory even three
4107	4	" memory odd three
4200	4	Exhaustive ECC verification, memory even zero
4201	4	" odd
4202	4	" even one
4203	4	" odd
4204	4	" even two
4205	4	" odd
4206	4	" even three
4207	4	" odd

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**NOTE All class 5 tests are CPU based. Similar to class 2.

5000	5	zone bit functionally
5020	5	test and set
5030	5	test and clear
5100	5	address = data single processor
5110	5	two processors
5120	5	multi processors
5200	5	MATS+, data pattern bits
5210	5	alternate data pattern
5220	5	data and ECC patterns
5230	5	ECC bit patterns
5300	5	data pattern algorithms
5310	5	alternate data pattern algorithms
5320	5	data and ECC pattern algorithms
5330	5	ECC pattern algorithms

This should get you started, for any more in depth questions, please contact the TAC.

Al,

2.36.1 Sabre Disk Part Replacements

When the Sabre series disk drives were first released to the field, it was described as a drive that would be field maintainable by replacement down to the FRU level. This has proved to be a great success both for logistics support and the field. Drives do not have to be completely replaced when one fails, except in a few minor instances, and this had saved a lot of customer down time now that file systems do not have to be reinstalled. This support activity will continue with all new Sabre series drives as they are released to the customers.

It is not required that an entire drive be returned to Dallas if one of the FRU's is bad. The failing FRU should be returned as a separate part while the rest of your spare drive continues to be available for spares. There have been instances of drives being returned to Dallas Field Service when only the drive control board is bad.

Kelvyn Gipp

2.37.1 C2/C3200 Power Supplies

As a reminder, the C2 wide body systems and the C3200 systems are shipping with the new HC power supplies. These silver colored power supplies are easily identified.

These supplies have a different master/slave relationship than the original LH supplies. When using the HC (silver) supplies, the "master supply" in the supply group is the one with the LOWEST voltage setting. This requires that all supplies in the supply group (including the master supply) be adjusted to the slave voltage point when a power supply is replaced. This must be done so the new supply can be adjusted correctly.

See Tech Tip "Power-006" for the correct voltage settings for these supplies.

Dave Muir

2.38.1 Disktab Entries for Sabre5 Disk Drives.

It is very important that the correct disktab entries be installed for the Sabre5 disk drives. The correct disktab entries can be found in Technical Bulletin V2W25

Due to an error in creating the tape for the ConvexOs 9.1 update tape, the incorrect disktab is included on the tape. If you have recently upgraded to 9.1 of the OS, it is very important to correct the disktab entries for the Sabre5 drives. If this is not done, file systems will be made using both the old and new disktab. This may eventually lead to difficult to diagnose system problems.

The TAC is presently looking into methods to examine the file system and determine which disktab was used to create it. This investigation should be completed in the near future.

Again, it is strongly recommended that /etc/disktab be checked on your next site visit to any site that has Sabre5 disk drives.

Dave Muir

2.38.2 dev_ultra diagnostic problem

The CONVEX diagnostic dev_ultra, subtest 201 (EPROM-based external loopback test) will intermittently report a "Loopback connector check failed" message during certain conditions.

After extensive testing this appears to be a problem that is caused by the test sequence only, but is aggravated by some transceivers. We have verified that H/W that fails in this way performs normally on the network and that it runs the dev_ultra diagnostic normally when the subtest sequencing is changed (see below).

CONFIGURATION INVOLVED

VME host adapter, CONVEX P/N 211-000108-200 Rev D, Ultra P/N 95-0032-001S or -004T

Any CONVEX supplied transceiver (coax or fiber)

CONVEX diagnostic dev_ultra.t 1.1

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RECOMMENDED DIAGNOSTIC WORKAROUND

This is a recommended change to the way the dev_ultra test is run. It is a temporary workaround that effectively tests the Ultranet H/W but avoids running the subtests in a manner that induces the "loopback connector error."

The board/transceiver can be tested using the dev_ultra diagnostic by running it in two phases against the H/W under test. In phase 1, subtest 100, 200 and 300 are run:

: test dev_ultra -s 100 200 300

This test should run indefinitely and without error on a good Ultra.

In phase 2, subtest 201 is looped

: test dev_ultra -s 201

Again, expect zero errors from a good Ultra.

Thanks to Russell Bleakley for this information

Rich Scheller

2.39.1 mm_sniff Failures During System Boot

It has been discovered that the combination of OSI WAN and Ultranet can cause mm_sniff to fail at boot.

What happens is that mm_sniff sleeps until a specific time during boot. When it wakes up, it expects certain processes and clocks to be completed and initiated. If the environment is not right mm_sniff will abort with a "68000 Dtack Timeout". This does not indicate any memory failure, but that mm_sniff was unable to start.

The combination of OSI WAN and Ultranet makes the kernel sufficiently large, that the environment is not right to start mm_sniff and so mm_sniff times out. So far, this is the only combination that has caused this failure, but there may be others, as all of the new products are released in the near future.

This problem has been identified and fixed. There is a patch available and this will be included in the 4.2 release of diagnostics. The correction will allow mm_sniff to sleep longer and therefore get past the problem.

If the patch is required, please contact the TAC.

Al,

2.39.2 Memory Configuration Rules

It should be noted that the rules on memory configurations have not changed with the release of MCM3. Odd size memory configurations will still not work properly.

All memory pairs should be the same size. If they differ in size, the memory will be configured in such a way that only the lowest common memory size will be used. This will mean that the customer is paying for unused memory.

For example; If you install 2 memory pairs, one at 128MB and one at 256MB then to protect interleaving, only 128MB will be used on the larger pair.

Again, it has always been this way and does not change with the MCM3.

Al,

2.39.3 New System Diagnostics and Diagnostic Database Release

As of 1 Nov. we will no longer issue a separate release for diagnostics and diagnostics database. The new release will be called Processor Diagnostics version 4.5. This next release will have support for new I/O products.

Al,

2.39.4 HiPPI - High Performance Parallel Interface

Another, new, I/O product will soon be introduced and will enter beta testing, at NCSA, on 30 Sep. This new product is called HiPPI (High Performance Parallel Interface) and is explained in this bulletin.

HiPPI is a new CCU designed for the I/O subsystem of the CXXX series systems. This includes the C2 class. HiPPI will not function on a C1.

The High Performance Parallel Interface (HiPPI) is the fastest industry standard interface for connecting high performance computers and their peripherals. This standard is relatively new, but there are numerous companies designing their own HiPPI product at this time.

The HiPPI hardware is a clone of the IDC/TLI hardware with the exceptions of a redesigned CPU area and HiPPI interface. Although, the software design is more like an EGOS kernel (IOP/VIOP) than it is an IDC Kernel. This allows for a kernel/driver format, with the initial driver being a HiPPI/UltraNet connection. This connection is to the Ultra Hub not the VME Ultra card.

Performance is expected to be in the 20 megabytes/second range, which is three times the performance of the current VME UltraNet. The HiPPI product is not expected to replace any existing CONVEX product at this time, including HSP and VME Ultra.

General Information

1) 32 bit implementation at CONVEX. (Standard permits 64 or 32 bit) Pbus is split protocol, HiPPI must emulate this protocol.

2) Can support 100MB burst between hub and CCU, but only 20MB on Pbus.

3) HiPPI is general hardware, based on same design as TLI/IDC. The software enables it to perform different functions. The only difference is HiPPI support for the receive/transmit side.

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4) The standard data cable can be removed from the Ultra hub and used for loopback purposes. This eliminates the need for a special loopback cable.

5) LED's (top to bottom)
   a) heartbeat
   b) idle
   c) 3 and 4 are for debugger use only.
   d) green is dead man timer (should be on)

6) Cables 3 60 pin and 1 40 pin. 40 pin is on rcv side and strips power. P4 & P5 is receive and P2 & P3 are xmit.
   a) Must use connector guides
   b) xmit and rcv cables must be crossed between hub and system. This means xmit cable to receive side and vise versa.

7) Hub
   a) Paddle cards xmit front and rcv back
   b) Two cards per link PP, protocol processor and hippi, or personality.
   c) loopback switch on hippi card on the hub. Light should be on. This switch will not allow a hub to HiPPI loopback test.

8) the ioconfig entry for hippi is

```
hippi <ccu slot number>
  drvr LAN-501
    unit 0 type HiPPI
```

9) Prerequisites
   a) software
      1) OS 9.1 and above
      2) Processor Diagnostic rev 4.5
      3) SPU Unix version 5.2
   b) hardware

1) VIOP	C2	rev F	C3	rev K
2) IDC	C2	rev S	C3	rev T
3) TLI	C2	rev F	C3	rev G

10) Diagnostic is hppi4000 and is similar in functionality to io5000, or idc4000.

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11) Part numbers

High Performance Parallel Interface	410-001328-200
HiPPI bulkhead I/F (Receive)	411-001322-200
HiPPI bulkhead I/F (Transmit)	411-002322-200
CCU to Bulkhead Cable (3 ea.)	604-600007-200
CCU to Bulkhead Cable (1 ea. 40 pin)	604-600005-200
External Cable (2 ea.) 25m	611-000119-003
External Cable (2 ea.) 15m	611-000119-002
External Cable (2 ea.) 5m	611-000119-001

NOTE The maximum cable length is 25 meters.

12) MANUALS
a) Service Guide DHW-281
b) Diagnostic Manual 760-003930-000

13) Training available on video, distributed to all regional managers.

Al,

2.39.5 IDCU Limitations in C210/C220

It should be remembered that no more than 2 IDC's can be installed in a standard C210, or C220 with 4 memory pairs. This is caused by limited power resources.

Al,

2.39.6 VIOP Revision Level for C3800 Systems

The VIOP must be at rev K to function on a C3800 system. This rev is downward compatible and can be used on all systems. In the future only this rev and higher will be issued through logistics.

As stated in a previous tech bulletin the appropriate C3 supported rev for TLI is G and for IDC rev T.
Changes have been made to the firmware that support the extended addressing use by the NIA in the C3800.

Al,

2.39.7 VME Versatec Interface Software Revision Level

The VME Versatec software displays a version header of V3.0 when installed. All the documentation shipped with the product is labeled as V2.1.

The documentation is correct for V3.0 and an ECO will be written to correct the mis-labeling between the software and the documentation.

Thanks to Bee-be Lindsay for this information.

Dave Muir

2.40.1 Status Code 07/Clock Problem Repair

As suggested earlier, in July 90, for front panel status codes of 07 (SM.SPUDCOK) the most common failed component, is the clock battery on the SP2, or SP4.

Now, in addition, it has been determined that for all date and time failures, such as slow clocks, or inaccurate dates, that the overwhelming solution has been to replace the battery. A defective clock battery should be suspected when encountering any of the above situations.

The battery is socketed and is located on the SP2/SP4 at location U065W5 in the lower right quadrant of the board. The part number of the battery is 166-001260-025.

Replacing this battery in the field can save CONVEX a great deal of money, as a date, or time problem is the most common symptom of returned SP2/SP4's.

Our thanks to Wes Mathies, of field service repair, for bringing this to our attention.

Al,

2.40.2 Fujitsu 3480 formatter power supply.

The initial shipments of Fujitsu 3480 formatters used jumpers to configure the power supply (described in the 3480 Cartridge Tape Drive Service Guide) for the A/C input voltage available.

The newer formatter power supply does not use jumpers. The power supply in these formatters is autoranging and does not require the setting of any jumpers.

Dave Muir

2.40.3 pia4000 Diagnostic Failure

Diagnostic pia4000 will fail subtest 300 if mcm-3 memory boards are used in the system.

This is a known failure, and should be corrected in a later release of the diagnostics.

Jerry

2.41.1 ps(1), W(1) and syspic(1) failures

In some instances, primarily after a new ConvexOS installation or upgrade, or after performing sysgens, the ps(1), w(1), and syspic(1) commands will fail with a message like:

```
mmap: can't mmap kernel virtual address 0 len 0
```

This is because the old ps files are still hanging around in the /lib directory. These old files should be removed:

```
convex# rm /lib/ps/ps.ttys /lib/kernsyms/symdata_*
```

They will be automatically regenerated when ps (or w or syspic) is next run. If you forget which files need to be removed, look at "man ps" under the "FILES" section.) If the problem persists, remove the files again and spu up the copy of vmunix you booted from. (The vmunix on the SPU and on the JP must match for the ps (and so on) commands to work.)

```
convex# mv /vmunix /vmunix.save
convex# spu -r /mnt/os/vmunix > /vmunix
```

The old ps files are what ps uses to keep track of what processes are run from which ttys and a copy of the kernel symbols and their addresses. If the addresses that ps thinks are correct don't match those of the spu:/mnt/os/vmunix you booted from, then the error occurs.

Josh Simon

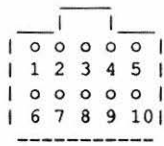
2.41.2 Fan Fail Sense Jumper

The fan fail sense jumper is required on widebody systems to disable the fan-fail sense board, or an individual fan. This is not required for standard C2's as there are pullup resistors on the SCM.

This jumper (p/n 603-010029-200) should be installed on the cable to the ESM and not on the sense board itself.

In the event that the jumper is unavailable, a 1K 1/4 watt resistor may be substituted and installed between pins 4 and 8 on the cable. The following diagram is with respect to the end of the cable:

.....continued on next page.....



Al,

2.41.3 Fatal Convex Unix Errors

With the release of 9.0 and 9.1 OS, we have begun to experience a Fatal Convex Unix that had previously been uncommon. This is because the new OS is causing previously known errors to trap in a slightly different place.

The error is a "pq_fm_alloc" and was previously reported as sync_deque, or RITA address and data parity errors.

This new crash is EFU/EDC related and has a, very, recognizable signature in the hardware dump. Essentially, one head appears to functioning normally as the other head/heads will spin on the same address. In other words, the same address will appear throughout the memory return queue, in register A5 and register T0.

If encountering this failure, please take a hwdump and contact the TAC, as this crash has been quite intermittent and nasty to identify, in the past.

Al,

2.42.1 HSP Troubleshooting Hints

The following are some hints for troubleshooting HSP problems. These should provide enough aid that further assistance will be unnecessary.

1) 95% of all HSP failures will be caused by cables, or cable configurations.

2) Any failure of class 4 of the diagnostic should be approached as a cable failure.

3) In situations where a short set of cables run fine, but the maximum 100' set will fail class 4 of the diags, this can be caused by shorted pins on the backplane, or the adapters. This is true because the HSP link to the HIA is differential, so there may be enough current to drive a short distance, but not enough to drive the 100'.

4) Verify that the proper power supply is installed in the system. The HSP draws more current on -5 VDC. More information on the power supply can be obtained from week 29's tech bulletin.

5) For long cable runs where the HIA is in a different room from the system, the grounds, particularly AC can be a problem, as the two may be on different power systems.

6) Customer designed boards should not be used to troubleshoot with, as timing problems could create problems for class 4 of the diagnostics. Instead the far side echo boards should be used for this effort. The part number for these boards are:

   a) Control card 410-001141-200; to be installed in slot 5 of HIA
   b) Buffer card 410-001142-200; to be installed in slot 4
   c) 2 foreplane connectors 410-000106-200 (each)

7) Manuals should be obtained before working on this subsystem. The part numbers follow:

   a) Farside Echo Test Procedure 900-000299-000
   b) HSP Users Guide 081-000110-000
   c) HIA Users Guide 081-000111-000

8) HSP is a standard product and is no longer supported by Special Systems. All requests for assistancei, for this product, should be directed to the TAC.

Al,

2.42.2 C1 Crashdump to SPU Tape

Because of changes made to support the 88K processors on the IDC, TLI, etc. it is now not possible to perform a crashdump to SPU Tape on a C1. This is because these changes were done with the knowledge of the windows available on a C2, but the C1 has fewer windows and thus exhausts its windows before the crashdump is complete.

The error will appear as follows:

```
Window allocate ioctl error
TERMINATED WITH ERRORS
```

This problem will be fixed as soon as practical. It is still possible perform a crashdump in this manner on C2's. In addition a standard crashdump to other tape devices will function properly on the C1.

Al,

2.42.3 DOA Definition

Due to the ambiguous present definition of what a DOA is and the problems this has caused in DOA analysis please use the following definition of DOAs, effective immediately.

A DOA is defined as a board that is DEAD ON ARRIVAL and/or fails before customer acceptance. Using this definition a spare that has previously been used to isolate a problem in another system cannot be considered a DOA. Only on the boards first use, can it be returned as a DOA.

INSTALLS - New system installation
If a board fails immediately upon installation or fails before customer acceptance of the product the board should be coded DOA.

FIELD SPARES - Field replacement
To help pinpoint DOAs, all board bags, as of 10/21/91, will now be sealed with a bar-coded label which will self-destruct when removed. This will indicate whether the board has ever been taken from the bag since it left Field Service Repair. Boards that fail after having been removed from a bag that has had the seal broken, should not be coded as a DOA, but as a normal failure. Please note on the P&A if the seal was broken.

.....continued on next page.....

Please address all questions concerning this subject to myself Rick Poole, (214) 497-4728, poole@-convex.com or Frank Fornara, (214) 497-4380, fornara@convex.com.

Rick Poole
Field Service Repair

2.42.4 ACL Software Problem

An error has been found in the Automatic Cartridge Loader (ACL) Software version 1.0 that affects dumps to any tape format. If the ACL software has been installed at any of your customer sites please have it removed as soon as possible and have your customers take new dumps as previous will be unusable unusable.

When the ACL software was installed it should have moved the old copy of "dump" to "dump1.0", so that returning to the old version of dump should be an easy process.

Kelvyn Gipp
Hardware Product Specialist
Technical Assistance Center
kgipp@convex.com

2.42.5 Console Reset Procedures

When a system crashes or hangs and the console also seems to hang, you might try one of the following methods to regain control of the console.

1. ^p
   <lf>
   <lf>
   reset<tab>tty<lf>
   <cr>

2. ^p
   power console off
   power console on
   type /etc/stty -raw<cr>
   <cr>

You should now have control of the console again.
Dan Brenner

2.43.1 EFU/EDC Failures

It is becoming increasingly apparent that many FE's are ignoring EFU/EDC related failures and waiting for their turn in the EFU/EDC upgrade program.

It needs to be understood that the known failures will not occur on a daily, or weekly basis. The time interval between crashes on the known ram parity errors, should be at least weeks apart and generally months between crashes.

If a system has been running with no failures for months and all of a sudden begins to crash frequently with 904/201 failures, this indicates that something has changed internally to the system. In other words, the system is broken. Making the customer wait for several months while they wait for the upgrade is not only unfair to the customer, but wastes company resources and damages our reputation.

Please understand, that 7 times out of ten the failure can be fixed on the spot and does not need to be placed on the waiting list, which in most cases will involve months of waiting.

This problem is going to be with us for several more years, so it's to everyone's advantage to learn to handle the failures as they occur. These problems can be solved and some effort should be made to do so.

Al,

2.43.2 MCM3 respin and DMM Release

We will soon release a new mcm3. This new board will will be a part number 3230 MCM3. The current board is a p/n 2230. This new board will have the identical functinality as the current 2230 MCM3. The only difference is that it will have a new DRAM controller installed, which will allow the board to utilize previously unusable 1MB DRAM's from Mitsubishi.

These mitsubishi DRAM's have not yet been released to the field, but will be when the 3230 MCM3 is released. After this board is released, the Mitsubishi DRAM's will be released on 2MB DMM's with a part number of 3204. These DMM's will be very easily identified, as they will have a label indicating 3204 affixed to the DMM. In addition there will be a yellow dot on the upper left corner of the DMM. The other DMM's (i.e. 0204 and 1204) currently have no identifying labels affixed.

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The one thing to remember is that the new 3204 DMM's can only be installed on the 3230 MCM3. The 3230 will be able to utilize all manufactured DMM's, while the 2230 MCM3 will be able to handle all but the 3204 DMM's.

Installing the 3204 DMM's on a 2230 MCM3 can result in noise related intermittent failures. This should be avoided at all costs and is the reason for the labels.

Al,

2.44.1 FDDI Product Release

We are about to release another VME based network product. This new product is FDDI (Fiber Distributed Data Interface). This controller has already entered beta test and should be released in December.

FDDI is a communications network that uses high-speed circuitry and fiber optic technology to achieve fast network performance. The FDDI product is designed to a maximum bandwidth of 100MBits per second and thus will be a faster solution to ethernet and far cheaper than Ultranet or Hyperchannel. The primary advantages of FDDI is the open standard and the price.

It is a high speed fiber optics network that outperforms ethernet by a factor of three (3). FDDI uses a token ring topology, so that all FDDI nodes are connected as part of the ring. In addition the product will be far more robust as the ring consists of 2 physical layers, a primary and secondary. The FDDI product will be VME based and will not be supported on multibus.

In addition an optical bypass switch (OBS) will be available from CONVEX as an option that will allow the ring to bypass the CONVEX in the event of a system shutdown. This will add to the reliability of the network.

External loopback tests can be run by means of a loopback connector and provided with each controller. This connector is then connected between the primary transmit and secondary receive lines. And then moved to check the secondary transmit and primary receive lines. This connector will allow the subsystem to be tested while keeping the ring alive. Class 2 subtests of the diagnostic will provide for this external loopback capability.

All external indicators will consist two leds on the controller, which is nothing more than an indication of successful initialization and self test completion.

The diagnostic for the VME FDDI controller will be called dev_vfddi. It will have similar execution format to that of existing VME controller diagnostic (dev5xxx). As with other diagnostics, it will require taking the system down to the dshell for execution.

The diagnostic will consist of 5 complete subclasses. The first are the low level functional tests. Most of these are firmware based. Class 2 will verify the data paths by loopback for both sides. Class 3 will consist of basic controller to VIOP command exchange. Class 4 tests will verify the FDDI's access to the ring. And Class 5 will test the controllers ability to access other nodes on the ring.

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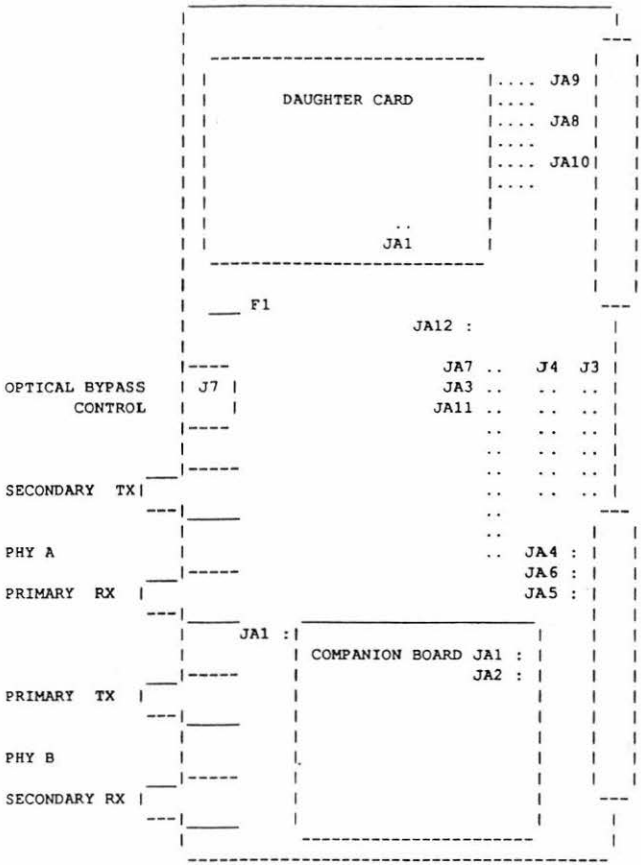
Part numbers for the major components are as follow:

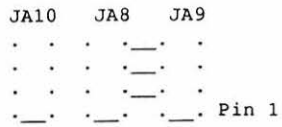
VME Host Adaptor	220-000021-200
Cables (2)	606-000001-001
Connector, loopback	312-000500-001



Jumper setting for csr address JA11:

```
Address Pin 7 Pin 6 Pin 5 Pin 4 Pin 3 Pin 2 Pin 1
6000      in    out   out     in    in     in    in
6200      in    out   out     in    in     in    out
```

Jumpers JA8, JA9 and JA10 are used to configure the BUS REQUEST level and should be configured for 3, as below:



Jumpers JA5 and JA6 will be used for the Optical Bypass control. Jumpers should not be installed as this will disable host control of the Optical Bypass Relay.

Because of the dual nature of the token ring, connectors are keyed to differentiate between the primary ring and the secondary ring. The standard calls for using red keys to identify the primary ring and blue is used to identify the secondary.

Al,

2.44.2 Unresolved Kernel pte Violation Troubleshooting

One of the more prevalent system crashes is the Fatal Convex Unix Error "trap: unresolved kernel pte violation". This failure can present a challenge to the FE because the failure can occur in so many different areas of the system.

This panic occurs as a result of an unresolvable virtual memory fault while executing in the kernel (i.e. within rings 0-3). The virtual address of the fault (as reported in A4 at the time of the exception) must also exist in rings 0-3. There are three basic causes for this exception:

1) The hardware generates a fault that is unnecessary, for example; a nonresident fault on a page that is resident, or the hardware incorrectly reports the faulting address (A4), or the trap code (A5). The A5 register will contain the exception trap code, with several codes indicating an, almost, 100% certainty of a hardware failure:

.....continued on next page.....

a) 0x00000C06 - Indicates an Invalid Thread Level PTE on a memory fault. This code generally indicates a problem in thread level, or parallel, area of a head. With this code the DC, or FU are strong candidates.

b) 0x00000C05 - Indicates an invalid level 1 PTE. This can indicate a scratch ram, or PTE cache failure. This will usually indicate a DC, or AS failure.

c) 0x00001001 - Indicates a non resident level 2 data page. This is almost always a DC failure.

d) 0x00001002 - Indicates a non resident PTET page. This will usually be a DC failure.

2) The hardware drops or adds bits while making a memory reference, causing a reference to the wrong address. Because the DC is responsible for the address interface to memory, it should be considered a prime candidate for the failure. It is also possible for the Utilities subsystem, or memory to contribute to this type of failure.

3) The kernel has a bug which causes an invalid memory reference. In this case the crash will be software induced.

The software should only be considered if the problem occurs directly after loading a new OS release, or a new application is being run for the first time that might cause the kernel to behave differently. If any of the above exception codes are seen, this problem should be considered a hardware failure. Almost all of these crashes that do not occur under the circumstances mentioned above, will be a hardware failure.

If one of the above codes do not appear in A5 after the exception, this does not mean that it is not a hardware problem, but if one of these codes is there, it always means a hardware exception.

Al,

2.44.3 New VIOP/VBCU for Real Time Systems

We will soon be releasing a new version of the of the VIOP/VBCU that is to utilized with real time operation. This board will be called the RTIOP. It is a faster version of the VIOP and will be almost identical in operation. It should be available in Q1.

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The Real Time IOP (RTIOP) is intended to address concerns about data transfer and system interrupt latencies associated with real-time applications. In order to address these concerns it is necessary to improve the performance of the VIOP in these areas. This is done by upgrading the 68020 from 20MHZ to 30MHZ to improve data throughput and additional hardware implementations to support this.

These additional hardware changes include decreasing the latency for inbound interrupts by decreasing 68020 overhead in the interrupt control path, use faster parts for the RAM and PAL's on the RTIOP and RTVBC hardware will be modified to allow the selection of bus arbitration. This last upgrade will allow the user, by software, to select priority arbitration over the standard round-robin method.

In addition, other enhancements under consideration include; Increasing VIOP memory size to 1MB from the standard 512KB and the inclusion of an interval timer on the board.

All of the above will be accomplished by upgrading the existing hardware. A respin will be accomplished at a later date. This product would be, primarily, directed at the P5300, P5400 and P5500 class systems.

There will be Standalone Diagnostics available for the Production Release of the RTIOP. This will be executed in a similar manner as the present I/O product diagnostics. The diagnostic will be designated io_rtiop. This diagnostic consists of an off-line functional test which can be executed from dshell.

This will be an enhanced version of the standard io5000 diagnostic, but will include logic to determine board type and if is determined to be RTIOP, it will run the real time based tests located in class 7 of the diag.

Part numbers for this subsystem include:

Real Time I/O Processor (RTIOP)	410-003149-200
Real Time VBCU (RTVBC)	410-002150-200
Cables (3 ea./VTVBC)	604-600001-201

Al,

2.45.1 New C3800 Flex Circuit Cables

Beginning with the DKRZ shipment, the dupont Flex Circuit (p/n 500-000326-200) cables will be replaced with epont Flex Circuit (p/n 500-000427-200) cables. This change will affect installations as the screw holding these cables in place will require a 5/32 inch hex socket that will fit into your torque screw driver. Also, the torque requirement for the epont cables is 8 inch pounds.

The 5/32 inch hex socket will be added to the C3800 tools being provided to the Field Engineers as they receive a system for installation.

Jerry

2.45.2 Fatal Convex Unix Error pq_fm_alloc error

We have recently experienced a new Fatal CONVEX Unix Error that has previously not been experienced. The format of the error is as follows:

"dsktypestrategy:pq_fm_alloc error"

* where dsktype will be da for MIOP, dd for VIOP, or du for IDC. This indicates the type of CCU that made the last request.

This failure indicates that the pbus is locked up and this particular disk subsystem is unable to access the MBS (Message Based System). This does not mean that the device that reports the failure is the device that has caused the failure. In most cases the opposite will be true.

A good test to run for this failure is io4000 subtest 200, or io5000 subtest 400. These are pbus interrupt tests and if the pbus is locked up, the offending CCU should fail.

So far, the indication is that a VIOP is the most likely candidate. But any CCU could generate the failure.

Al,

2.45.3 PDU in EXP-105 Cabinets

Some of the early versions of the EXP-105 PDU were assembled differently than the current production units.

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The older version had the sense input connectors rotated 180 degrees from the current configuration.

Note that the only difference is in the way the 4 pin connector was inserted in the chassis.

Some documentation may incorrectly state that all unused sense inputs must have pins 1 and 3 jumpered together. As you can see from the above diagram, the unused inputs must have pins 2 and 4 jumpered together regardless of the connector orientation.

Dave Muir

2.46.1 Loopback cable for dev4540 diagnostic

For all of you X.25 users, the following describes the requirements to build an RS232 Loopback Cable. This cable is required for a complete diagnostic test.

4 RS232 25 pin Male connector.
16 lengths of wire.

Each connector should be wired as follows:

```
2 <--+
     |
3 <--+

4 <--+
     |
5 <--+

6 <--+
     |
20 <-+

17 <-+
     |
24 <-+
```

Kelvyn

2.46.2 GIP Software Tapes

Convex has recently begun shipping software on GIP format tapes. This allows multiple software products to be stacked on a single tape. Use care not to lose the envelope with the gold "CONVEX SOFTWARE" label attached when unpacking software shipments. This envelope contains a list of software products on each tape and the software activation keys for each product.

This software list and the corresponding tape should identified and marked. There is currently no way to identify which list belongs with which tape if they become separated.

In the near future, the tape and the corresponding software list will be marked for identification.

Dave Muir

2.47.1 C1- Can Not Use MAU7 and MAU6 for CCU Slots

C1 systems CAN NOT use FM0048 (ECN 102195) to allow the MAU6, and MAU7 slots to be modified to be used as CCU slots. Too many changes will need to made to accomplish this change, far more than the one quoted in the FMI.

There are also NO engineering plans to attempt this modification.

Kelvyn

2.47.2 C2 Backpanel Pin Locations

This is a reminder of how the backplane pins are layed out on "C2XX" Machines. Please make a note of it.

HDI PIN LAYOUT

Each HDI connector has 300 "Main" contact pins, positioned in 4-columns of 75-pins each. These pins are identified by either the "total count" method or by the "column / row" method.

In addition to the Main Pins, each HDI connector has 30, 3-pin sets of "auxiliary" contacts. 15, 3-pin set are located on each side of the main contact-pins. These pins are identified as column 5, VOLTAGE(left column) and column 6, GROUND (far-right column).

.....continued on next page.....

```
Columns:   1234        REAR of BACKPLANE
Columns:  5||||6
          ||||||
  Row 1:   ....    Pin #:       101, 201, 301, 401.
           ......  Pin #: 502, 102, 202, 302, 402, 602.
           ......  Pin #: 503, 103, 203, 303, 403, 603.
           ......  Pin #: 504, 104, 204, 304, 404, 604.
            ....   Pin #:       105, 205, 305, 405.
  Row 6:   ....    Pin #:       106, 206, 306, 406.
           ......  Pin #: 507, 107, 207, 307, 407, 607.
           ......  Pin #: 508, 108, 208, 308, 408, 608
           ......  Pin #: 509, 109, 209, 309, 409, 609.
            ....   Pin #:       110, 210, 310, 410.
 Row 11:   ....    Pin #:       111, 211, 311, 411.
           ......  Pin #: 512, 112, 212, 312, 412, 612.
 Row 13:           Pin #: 513, 113, 213, 313, 413, 613.
    |
 (thru)                 - - - - through - - - - -
    |
 Row 66:           Pin #:       166, 266, 366, 466.
 Row 67:   ......  Pin #: 567, 167, 267, 367, 467, 667.
           ......  Pin #: 568, 168, 268, 368, 468, 668.
           ......  Pin #: 569, 169, 269, 369, 469, 669.
            ....   Pin #:       170, 270, 370, 470.
 Row 71:   ....    Pin #:       171, 271, 371, 471.
           ......  Pin #: 572, 172, 272, 372, 472, 672.
           ......  Pin #: 573, 173, 273, 373, 473, 673.
           ......  Pin #: 574, 174, 274, 374, 474, 674.
 Row 75:   ....    Pin #:       175, 275, 375, 475.
```

This figure represents only the beginning and ending connector. Remember that rows 5xx are voltage pins and rows 6xx are ground pins.

Thanks
Rick

2.48.1 Happy Thanksgiving.

Due to the abreviated work week, there are no technical articles this week.

Dave

2.49.1 VASYNC/Printer Panel Assembly

It has been found on some shipments of VASYNC/Printer Panel Assemblies, that the DC/DC converter has moved in the securing strap and now provides intermittent power, and thus problems, once installed at a customer site. This problem has been resolved in newer assemblies by the soldering of the DC/DC Converter onto the printed circuit board that is part of the VASYNC/Printer Panel Assembly.

Kelvyn

2.49.2 VMEbus Versatec Hardcopy Interface Manual Error

It has been brought to our attention that the Configurator for the VMEbus Versatec Hardcopy Interface (Convex P/N 211-000111-200) is incorrect. This document is provided in the Tech Tips, GEN-011 Pages 92 & 93.

On page 93, the BASE ADDRESS SWITCH SETTINGS are backwards; all that say 'OFF' should say 'ON' and all that say 'ON' should say 'OFF'. This error extends to the information for U54 switches 5-8 as well.

Also, if the need arises to have more than one VME Versatec board in a VME chassis, subsequent controllers should be addressed 0x0010 above the first board. For example, if the csr address of the first board is 0x0100, the second controller's address switches would be set to 0x0110.

The configurator will be ECN'd and the Tech Tip changed to reflect the correct information. The CONVEX VMEbus Versatec Interface Installation and Maintenance Guide, Document No. 081-007830-000, is correct as written.

Many thanks to Ronald Ophof, FE / Holland, for bringing this to our attention.

Dan Schoner

2.49.3 New C2 Front Panel Menu

We have a new SPU firmware release for the C2 that changes the behavior and display characteristics of the front panel. This new firmware is implemented on the SP4 rev M and the SP2 rev T.

.....continued on next page....

One new option of the new frimware is to allow the setting of the delay time for the first access to the spu disk. This option is called "SCSI-power-up- delay" and is set in seconds. The default for this is 0, or no delay which can cause the SPU to access the disk before it is ready. This will cause the SPU to appear to hang. The proper delay for this entry is 5 and can be set by entering "S=5" at the (fp)>.

The new front panel display is shown below:

```
CONVEX Front Panel - Version: 3.32 / CPU Class: 7 / CPU SN 32514
SPU type = SP5                          Processor = 68000
mode-of-operation = normal-os           boot-device = disk
location-of-bootstrap = default         power-up-reboot = enable
automatic-reboot = enable               spu-selftest = enable
test-flags = normal                     remote-port-bps = 1200
SCSI-power-up-delay = 0x5               user-flags = 0x0
(fp)> b
```

Al,

2.50.1 DAT Tape Drive Manual

It has been found that the "Product Description Manual" for the Archive DDS DAT Tape Drive has an error in it. The error appears in manuals prior to November 1990. The error is on page 39 which incorrectly shows the positions for the "write protect/enable tab" on the DAT cassette. The picture on the left of Figure 18 should be labeled "WRITE ENABLED", and the picture on the right of Figure 18 should be labeled "WRITE PROTECTED".

Manual Part Numbers 25354-001 and -002 are in error. Manual Part Numbers 25354-003 (November 1990) and later are correct.

Please correct all copies within your area.
Kelvyn

2.50.2 Fan Kit Assemble for EXP-101 Cabinet

I am in the process of releasing a HPPC type of Fan Assy Kit with rear door and cables. This kit is to be used in the C1 & early non-HPPC C2 peripheral expansion cabinets. Due to the additional cooling this fan package offers, the customer will be able to load more devices into the peripheral cabinets thereby giving the customer's i/o system more capacity (up to 24 amps).

Further, if the customer ran out of power outlets on the power controller, the customer could purchase his own power outlet strip which he would plug into one of the power controller outlets in order to gain several more power outlets. This power outlet strip would need to be the type with a circuit breaker on it in order to help identify the outlet strip as the source of the power failure in the event the customer over loaded the power strip. In other words the customer would have to stay within the current loading limits of the power outlet strip as well as within the 24 amp limit of the power controller in each expansion cabinet.

The major differences between the HPPC and this package is:

1) 24 amp (vs 48 amp capacity on HPPC system)
2) Non-Hall-Effect fans (vs Hall-Effect fans on HPPC system)
3) Non-Logic control (vs Logic control of fans on HPPC system)

NOTE: This fan will be available in two packages as follows ...
1) KIT, FAN 125V 600CFM C1/C2 PERIPH C 550-003863-200
2) KIT, FAN 230V 600CFM C1/C2 PERIPH C 550-003864-200

Thanks to Richard Prahl for this information
Dave Muir

2.51.1 FMI 0089 dev_vscsit expected failures

Please be aware that after installing FMI 0089 on the VME SCSI Host Adapter the following sub-tests of dev_vscsit will fail:

200 Tape Controller Self-Test
400 Beginning-of-Tape Exception Test
402 End of Data (EOD) Test

The diagnostic dev_vscsit has been rewritten to recognize the new firmware, and is available by ordering ACL V1.1 from Judy Palma or Jim Meade. Those of you who are installing the Stackers on SCSI 3480's will receive this software with the Stacker/Loader upgrade.

Thanks to Dan Page who discovered that the older diags fail, and my apologies to the Field for not putting this information in the FMI.

Dan Schoner

2.51.2 FMI0089 call for Information

Several people have informed me that their sites did not show up in the effectivity list for FMI0089. This list was generated from a search of the 'STARS' database, keying on the part number for the SCSI Host Adapter. Of particular interest are the sites sold or maintained by distributors - records seem to be incomplete or inaccurate. If you know of a system that has a SCSI Host Adapter that did not show up on the FMI, please send me e-mail with the System Serial Number, quantity of SCSI Host Adapters, location, and if available, a recent cop.out. I'll forward the information to the appropriate folks.

Dan Schoner

Since this is the last bulletin before Christmas, I will take this opportunity to wish you a happy and safe holiday season from everyone in the TAC.

Dave Muir

TECHNICAL BULLETIN

Volume Number: 2

Week Number: 52

Due to the holidays there are no technical bulletins this week.

Have a happy New Year.

Al,

3.1.1 ESM, ESMI and JSM build changes

Convex used to build 3 different system monitor boards for C2XXw, C2XXi and Javelin systems. The main difference is the EPROM on the boards.

ESM 410-001180-200 was for the C2XXw.
ESMI 410-002180-200 was for the C2XXi.
JSM 410-003180-200 was for the Javelin. (standard and Jr.)

Convex has decided to build only the 3180 without the EPROM. The 3180 with the proper EPROM can replace the 1180 or 2180. This will allow us to build and stock fewer board variations.

The Javelin and Javelin Jr. systems must use the 3180.

You will need to order the correct EPROM when you order a system monitor board for a C2XXw, C2XXi or Javelin system.

Current shipable EPROMs are:

181-030017-111 or 112 for the C2XXw.
181-030040-105 for the C2XXi.
181-030041-107 for the Javelin and Javelin Jr.

If you order a 3180 and not the EPROM, you should be able to use the EPROM from the board you are replacing. Failure data has shown very few EPROM related monitor board failures.

Dan Brenner

3.2.1 780mb RDS disktab With ConvexOs 10.0

Before you upgrade any system with DKD-284 disk drives, check the /etc/disktab on the system disk. There is a change in the dikstab supplied with 10.0 of the OS. This change will affect filesystems created with 10.0 on either a C or H partition. In either case, it will necessary to dump the data from the disk, do a nfs and then restore the data.

You man not see any adverse affects on the system unless either the C or H partition is getting very full, then you may see "end of medium" or other similar errors due to the difference in the partition size.

You may have the following disktab:
/etc/disktab for 8.1 and 9.1 systems

```
dkd-284|DKD-284|Vrds780|Hitachi 515-78 on VME:\
        :ty=winchester:se#512:ns#68:nt#14:nc#1361:rm#3600\
        :pa#64640:ba#8192:fa#1024:\
        :pb#258944:bb#8192:fb#1024:\
        :pc#1287936:bc#65536:fc#8192:\
        :pd#64640:bd#8192:fd#1024:\
        :pe#388352:be#4096:fe#512:\
        :pf#129408:bf#4096:ff#1024:\
        :pg#582528:bg#4096:fg#512:\
        :ph#381696:bh#4096:fh#1024:
```

The following is from a 10.0 system:
/etc/disktab for 10.0

```
dkd-284|DKD-284|Vrds780|Hitachi 515-78 on VME:\
        :ty=winchester:se#512:ns#68:nt#14:nc#1360:rm#3600\
        :pa#64640:ba#8192:fa#1024:\
        :pb#258944:bb#8192:fb#1024:\
        :pc#1287040:bc#65536:fc#8192:\
        :pd#64640:bd#8192:fd#1024:\
        :pe#388352:be#4096:fe#512:\
        :pf#129408:bf#4096:ff#1024:\
        :pg#582528:bg#4096:fg#512:\
        :ph#380800:bh#4096:fh#1024:
```

Dave Muir

3.3.1 Insulated Replacement Pins For C2/C3200 and C3400 HDI Connectors

There is a new insulated pin (314-000121-500) that can be used on the C2/C32 series processor, and MUST be used as a replacement pin on any C3400 series processor. The new pin appears the same as previous pins, but the insulation extends further along the body. This is needed since the C3400 backplane is slightly thicker than the C2 backplane. Using the older style insulated pins (314-000120-500) will result in shorted nets if used in a C3400 backplane.

Dave Muir

3.4.1 Sabre 7 Disk Drive Answers

SABRE 7 disk drives are becoming a very popular product with our customers. The following information is provided to assist with customer questions.

1. The SABRE 7 drive can only be used with OS 9.1 and above.

2. The IDC V5.0 s/w must be installed for these drives to operate with OS 9.1.

3. The full "C" partition of this drive cannot be used until the customer system is running OS 10.0. This is because it will currently exceed the file system size restriction under OS 9.1.

4. If the initial install of OS 9.1 is done with a SABRE 7 drive as the root disk, you must install the SABRE 7 Software V1.0 in addition to IDC V5.0 software.

5. Spindle sync on the DKD-503/504 drive is not supported. The drives have the capability to have sync cables connected, but this has been found to provide no performance benefit, and is thus not recommended. All drives shipped have this function disabled on the I/O board, and no cables or terminators are supplied.

Kelvyn

3.4.2 OPUS Memory Component Identification

When encountering a memory error during self test the OPUS workstation for the C3800 does not directly display the failing module. This bulletin should help in isolating the failed component.

The normal error on the OPUS will be of the type BxBy where the relationship to possible simms is shown in the table below:

.....continued on next page.....

x,y	SIMMS
0 0	MR8, MR4, ML8
0 1	MR7, MR3, ML7
0 2	MR6, MR2, ML6
0 3	MR5, MR1, ML5
1 0	MR8
1 1	MR7
1 2	MR6
1 3	MR5
2 0	ML4
2 1	ML3
2 2	ML2
2 3	ML1
3 0	MR4
3 1	MR3
3 2	MR2
3 3	MR1

In cases where further isolation is necessary it will be necessary to use the physical address. The physical address can acquired from the syslog file located in /var/adm/messages. The format of the entry for the memory error is as follows:

date time info: pme=nnnnnnnn,phys addr=wnnnnnz

This physical address is only necessary is the the x value is 0 in the error display BxBy. If this is the case then use the following table:

phys addr	x,y	SIMM
nnnnnn	0 0	ML8
where leading 0	0 1	ML7
is dropped in 7	0 2	ML6
digit addr.	0 3	ML5
1nnnnnn	0 0	MR8
where addr has	0 1	MR7
leading 1	0 2	MR6
	0 3	MR5

.....continued on next page.....

3nnnnnn	0 0	MR4
where addr has	0 1	MR3
leading 3	0 2	MR2
	0 3	MR1

If, for some reason, the error message is not displayed, the faulty SIMM can be isolated from the physical address as follows:

phys addr	where z =			
	0,4,8,c	1,5,9,d	2,6,a,e	3,7,b,f
nnnnnz leading 0	ML8	ML7	ML6	ML5
1nnnnnz	MR8	MR7	MR6	MR5
2nnnnnz	ML4	ML3	ML2	ML1
3nnnnnz	MR4	MR3	MR2	MR1

Here are some examples:

EXAMPLE 1:

```
   Phys Addr: 1394CA8
              ^^    ^
              ||    |__ 1000
              ||        ^^
              ||        ||__ 00
              ||_____________ 01nnnnnn
```

SIMM: MR8

EXAMPLE 2:

```
   Phys Addr: 3381AB8
              ^^    ^
              ||    |__ 1000
              ||        ^^
              ||        ||__ 00
              ||_____________ 03nnnnnn
```

SIMM: MR4

.....continued on next page.....

EXAMPLE 3:

```
   Phys Addr: 32A0204
              ^^     ^
              ||     |__ 0100
              ||        ^^
              ||        ||__ 00
              ||_____________ 03nnnnnn
```

SIMM: MR4

Al,

3.4.3 C3 PETS Problem

When executing PETS on a C3 system it is possible to encounter a Bus Error while attempting to execute run96. This can occur because a defective csh is shipped on the system. This problem can be remedied by going to single user and saving the file /bin/csh and copying /bin/oldcsh to /bin/csh.

This problem is being pursued and should be corrected shortly.

Al,

3.4.4 C201 to C210 System Upgrade

The following are a rough outline of procedures for upgrading a C201 to a C210 system.

a) Obtain a new serial number from marketing

b) Order new serialized software

c) Replace CPX with part number 2201, or 4201

d) Replace PIA with part number 2212

e) Install mode jumper on J10 on 135 SCM, or J9 on 168 type SCM. Without this jumper, system will fail with status 0B.

f) Change serial number on backplane. This is quite easy and should be remembered that the jumpers on the backplane are binary weighted and removing the jumper makes the bit high. The connector J13 is weighted right to left and should appear as follows.

.....continued on next page.....

```
| | | | | | | | | | | | | | | | |
  1 2 4 8 1 3 6 1 2 5 1 2 4 8 1 3
        6 2 4 2 5 1 0 0 0 1 6 2
            8 6 2 2 4 9 9 3 7
                  4 8 6 2 8 6
                        4 8
```

For example: For serial number 8648, remove the following jumpers,

```
8192
 256
 128
  64
   8
----
8648
```

g) Load new serialized software

Al,

3.4.5 C2 Power Plug and Receptacle

We are now shipping two manufacturers versions of the C2 power plug and receptacle. The original one being hubbel and the newer one be produced by the German firm Meneke. Because of this, it is not possible for a domestic customer to locate the proper receptacle conduit adapter for the conduit used in the installation.

Because of this, it is necessary to try and insure that only hubbel connectors are distributed to C2 system customers. At current the part number 303-000026-002 includes both manufacturer's parts and so there is little control over the connector and receptacle sent.

The plan is to break these two parts out and to have separate part numbers to order by. Until this takes place it will be necessary to notify the TAC when these connectors are being ordered and for us to try and hand pick the parts.

Al,

.....continued on next page.....

3.4.6 VME Ethernet Jumpers

Before returning a VME ethernet controller as DOA, please verify that jumper J15 and J9 are in the right locations for the firmware installed. For 5.5 firmware J15 should be installed between pins 1 and 2 and J9 should be removed. For 6.2 firmware J15 should be installed on pins 2 and 3 and J9 should be installed.

These ethernet controllers have appeared in the field with only the EPROMs changed without the necessary strapping.

Al,

3.4.7 C3 Bay Configuration Considerations

Although there is no functional reason that the C3 bays cannot be configured in any manner, or combination necessary, there are several considerations that should be addressed prior to using a nonstandard bay arrangement:

1) It would be difficult to determine the exact physical configuration when dialing in by personnel not familiar with the site. This could lead to less than optimum troubleshooting decisions.

2) Although all ports will be tested, the most thorough testing will generally occur while configured in the standard manner.

3) If the configuration is done purely for appearances, then when upgrades are performed, it may be necessary to reconfigure the entire system again. This can result in introducing additional failures and increasing the work load.

By considering the situation from this perspective will lead to a more satisfied customer and Field Engineer.

Al,

3.4.8 C3 I/O Bulkhead Boards

It has been decided that CONVEX will begin shipping I/O bulkhead boards in all slots on all C3 shipments.

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In the past only the bulkheads for the required configuration were being shipped. This meant that the cables were run from the CCU's and tied up where they would attach to the bulkheads. This could cause some difficulty when it was necessary to upgrade the I/O on the 3800.

This means that all unused slots will contain IDC bulkheads, as this is the most likely upgrade path to be selected by a customer. If a different bulkhead is necessary then it will be replaced for the one installed and the IDC bulkhead returned.

It is hoped that this will make future upgrades easier for the field.

Al,

3.4.9 VME Controller Interrupt Level Selection

As a rule of thumb, most VME controllers interrupt levels are software selectable. This means that the interrupt level is set in the ioconfig entry for the device and then downloaded at boot.

The exceptions to this rule are the ethernet, tape and versatec controllers. These devices still use jumpers on the board to indicate and change the interrupt level of the controllers. These controllers are some of the oldest VME devices used and this is why the jumpers are still used. All new controllers will use the software selection method.

The bus request/bus grant jumpers should not be confused with the interrupt level as these perform totally different functions and the bus request is still jumper sealable on all controllers. Bus Request level 3 is generally used for CONVEX VME devices.

Al,

3.4.10 C3800 Transformer Requirement

CONVEX has decided that the transformer is absolutely necessary for all 3800 installations. Mechanical Engineering feels that this is necessary for the following reasons:

1) The FCC validation was received with a transformer in the configuration. So, it is necessary to maintain this validation.

2) For impedance matching between the AC source and the system.

3) For phase balancing within 5%.

.....continued on next page.....

Again, it should be explained to the customer that this transformer is a requirement for a C3800 installation.

Al,

3.4.11 C3 Purge Ram Function

There have been numerous questions regarding purge rams and this will be an attempt to shed some light on the subject.

The purge rams are a mechanism of the Neptune cache system that is used to track the use and validity of the individual cache data. These purge rams are very similar in function to the Tag and Validity Rams that are used in the C2 RITA circuitry. The major difference between the C2 and C3 are that in the C2 individual invalidation and replacement was used in the cache, but in the C3 the entire cache is purged. The purge operation will be performed in one clock cycle.

All purge rams are located on the NSP and there are 19 of these devices located on each NSP.

These purge rams can be identified as any net or signal that contains a reference to tag, validity, update, or history. For example: the error npa1.pval_par_err is an example of a purge ram parity error. Note the second entry pval contains the reference to validity.

Al,

3.4.12 C3 With OPUS Console

Now that the OPUS is now shipping as the console device for C3's it is important to understand that the NWI (Neptune Workstation Interface) has been replaced by the SWIP and SWIS boards. The SWIP is the parallel interface to the system, which attaches directly to the NCU on the backplane. The SWIS is a serial interface used for communication with the power subsystem and attaches to the central cabinet distribution board.

To verify connection for the parallel cable, it should be noted that a jumper exists between pins 1 and 100 on the backplane. If the cable is installed correctly the resistance between these two pins should measure as a short. Pin 1 on the connector is the upper left pin of the connector and pin 100 is in the lower right position.

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There is a new display used with the OPUS that can come in handy. This command is "dump_swip". When entered, this will display the contents of various registers on the SWIP as follow:

swip_bsrc_msb:	16*10
swip_bsrc_lsb:	16*10
swip_force_par_err:	16*00
swip_misc:	16*80
swip_int_level_ctl:	16*90
swip_int_ena:	16*40
swip_int_stat:	16*00
swip_force_int:	16*00

The contents of these registers should appear as above. If they have other bits set, it is possible that the system will be unable to boot and generate a "NCU Bus Error". If this occurs it will be necessary to manipulate the registers to the values shown above. For example:

put swip_force_par_err 16*00

If the register does not change run "cleanup" and reissue the put command.

This process can be followed for any register shown above.

Al,

3.4.13 C3400 I/O Connection

There has been some confusion on connecting I/O device to the javelin backplane. The I/O slots in the javelin are identical to the C2 product line and all i/o connections are made the same way using P2, P3, and P4.

Since all iop's used in javelin are VME type, the brown wire of the vbcu cable is up for the 'x' side and down for the 'y' side of the connector.

Dave

3.5.1 3480/ACL Upgrade

Once an ACL upgrade has been installed on a system that has 3480 Tape drives, the old peripheral cabinet door should not be returned to Dallas. It can be retained by the customer, or local field office, as a souvenir, a spare, or whatever. Just don't return it.

Kelvyn

3.5.2 C3800 Gate Array Functions

The following are a list of gate arrays used in the C3800. Included will be a short functional description and in parentheses will be the number installed on that board.

Located on NVP

NVD (1) Vector Dispatch -- Vector Dispatch logic receives instructions from the IP on the NSP.

NIS (2) Input Staging -- The Input staging gate arrays handle data from the NSP and memory. Referred to as IS0 and IS1.

NVRF (8) Vector Register File -- Eight 128X64 vector registers labeled V0-V7. Same as C2.

NVM (3) Pipe Controllers -- Controls Add, Multiply and Load pipes.

NQ (3) Pipe Control Queues -- One for each pipe.

Located on NSP

In NAS Section (Address and Scalar Data Path)

NUS (1) Micro Sequencer -- Controls AS. Converts instructions from IP to microinstruction stream for execution.

NRFA (4) Register File -- Main Integer execution unit. Contains

8x32 Address registers	(A0-A7)
8x64 Scalar Registers	(S0-S7)
8x32 Temporary Registers	(T0-T7)
Hazard Logic	

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NPSW (1)	Program Status Word -- Controls flow through functional Units.
NMISC (1)	Miscellaneous Functions -- Floating point to/from integer conversions. Leading ones, trailing zero, shift and population count.
NFAD (1)	Floating Point
NMUL (1)	Floating Point Multiply
NDIV (1)	Division and Square Root
	In NIP (Instruction Processor)
NIAD (2)	Instruction Processor Address Generation -- Address
NPAR (1)	Instruction Parser -- Cracks Entry Points, register fields, and other info from the Icache.
	In NDC (Data Cache)
NDC (1)	Data Cache Control
NDP (3)	Data Path -- Stages data for the DC
NAG (2)	Logical Address Generation -- Stages Addresses for the DC
NPA (2)	Physical Address Generation -- One even and one odd.
	In NRC (Return Control)
NRC (3)	Return Control

AI,

3.5.3 FDDI Configuration Information

The cable spec for FDDI configurations is 62.5/125. Other cables can be utilized with the understanding that the signal loss will increase. The maximum distance between nodes, using this fiber, is 2 km.

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The connector types are as follow:

ST to FSD cable	AMP 502125-7
FSD to FSD cable	AMP 502122-7
Optical Bypass Sw.	AMP 501916-2
Optical Bypass Control	SA39

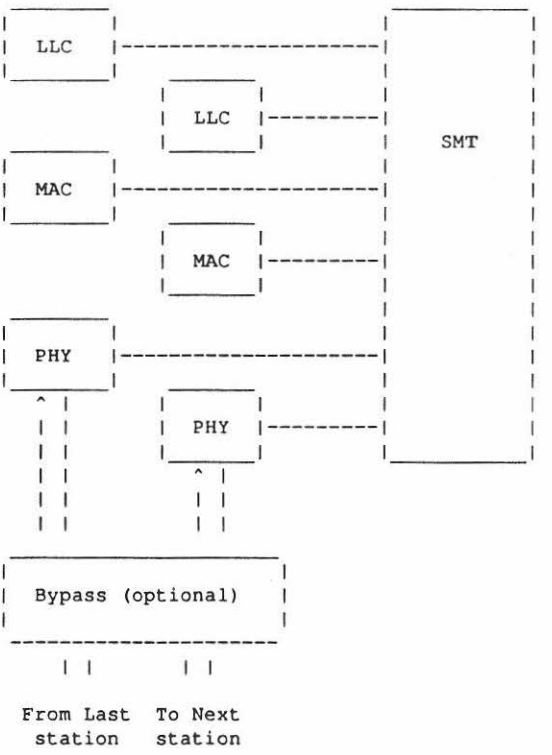
The optical Bypass switch is optional and is used to bypass the system when it is down.

The normal configuration is a dual attach configuration, but can be configured in Single fashion for going to a concentrator.

The following are examples of single (concentrator) and dual attachment station configurations for FDDI:

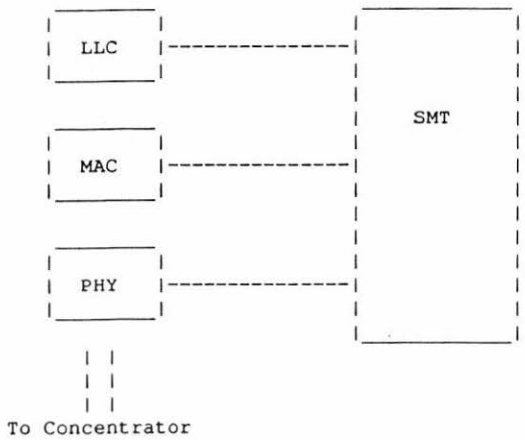
.....continued on next page.....

DUAL ATTACHMENT STATION



.....continued on next page.....

SINGLE ATTACHMENT STATION



Where LLC = Logical Link Control Implementation
MAC = Media Access Control
PHY = Physical Layer Protocol
SMT = Station Management

Al,

3.5.4 C3800 Software Upgrades

New software has been sent to the field for the C3800. This software includes some diagnostic fixes, patches and special dumpers to gather more information on known problems. The new software is:

760-004315-000	SpuOS X1.0.0.1 Opus
710-010915-005	ConvexOS V10.0.2 Opus
760-003615-00X	3800 SYS DIAG X1.0.0.5

.....continued on next page.....

In the way of diagnostics. All work except cpu4333. Diagnostic cpu4332 will run but fails subtest 211.

The date can now be changed in the SPU window with the OS booted. The console printer will now work as intended.

The new dumpers will be executed by the hard_logger when the particular crash is encountered. The output of these dumpers will not be saved in the errlog but will appear in output files in /users/diaguser as follow:

1) For purge ram errors 2 files are generated. pram.log.'date' & pram.stdout.'date' where date is the actual date.

2) For nrvf failures the file is nvrf.out.'date'.

3) For dcache stram failures the file is dcache.out.'date'

4) For icache stram failures the file is icache.out.'date'

5) For ptecache stram failures the file is ptecache.out.'date'

After a crash involving one of the above, it will be necessary to forward the contents of the appropriate file and the errlog to the TAC as soon as possible.

Al,

3.5.5 Dialing Into an Opus Workstation

The following is a detailed description for dialing into the Opus Workstation on a C3800.

With key-switch is in REMOTE-POSTION:

Do a "tip" to the OPUS for dialing into the Opus-workstation and login as rmtdiag user. This will log you onto the OPUS.
When you want to go to CONVEXOS do a <cntr>D and a <RTN> Then you will get the CONVEXOS login prompt.
Log in as CONVEX user on CONVEXOS.
After finishing logout and do a <cntr>P twice to go back to the Opus-workstation and enter "remote-disconnect" which will hanging-up the line.

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When in SECURE or LOCAL-POSITION:

Do a "tip" to the OPUS for dialing into the Opus-workstation and you will be linked directly to the spu window and log in as diaguser. Logging in as rmtdiag will disconnect you directly. None of both positions will give you permissions of logging in onto the CONVEXOS environment.

Geert Burgler FE Convex, Netherlands

3.5.6 C3800 system Diags Rev. X.1.0.0.5

With the system diagnostic rev x1.0.0.5, the printer will now function on the Opus workstation of the C3800.

The printer will echo everything on the convexOS screen when the printer switch is toggled in the soft front panel display.

When attempting to print a file it is necessary to move the cursor to the proper screen and "cat <filename> > /dev/prt".

Al,

3.5.7 Loading C3800 SPU OS

It is possible, when loading new SPU OS, for the oscillator frequency to be reset to default on the C3800. The default at current is 18ns, so it may be necessary to reset this after loading new software.

To reset the oscillator frequency the following procedure can be used:

1) The file "osc_update" should be modified for the desired clock speed, where the value 0 is for 18ns and default and "2" is for 16.7ns. The file osc_update is located in /diag/db.

2) After modifying the file osc_update it is then necessary to execute is file and that will permanently set the clock speed.

3) To verify the clock it is necessary to display the sys config window under the xtools display.

Al,

3.5.8 C3800 PETS

The PETS executed on a C3800 is not the same as that previously used on the C2.

The C3800 version is in a state of flux and is in the process of being ecn'd, so it can be distributed to the field. In the mean time each tape must be generated individually and must be ordered thru the TAC.

The C3800 version of PETS is not in installsw format, but is currently only in tar format.

Al,

3.5.9 OPUS Software Revision Infomation

To locate the revision levels of current software on the OPUS, list the following files:

/SPUOS_REV
/diag/DIAG_REV
/mnt/os/VMUNIX_REV

Al,

3.5.10 Avoiding C3800 OPUS Workstation Reboots

It should be understood that the nature of the workstation to C3800 interface makes the OPUS somewhat unstable and abnormal faults, or reboots can cause the swip to hang. This is the nature of the configuration and should be approached as a sysreset for a failed system would be. The problems should not even require a reboot.

I am resending this bulletin with the hopes that most workstation reboots can be avoided. If the system seems to act strange and won't allow, even a sysreset, or generates "clock generator busy" messages when attempting something, this means that the swip is hung up. To unhang the swip, it is only necessary to enter "cleanup" and follow this procedure to clear up any remaining problems.

Now that the OPUS is now shipping as the console device for C38's it is important to understand that the NWI (Neptune Workstation Interface) has been replaced by the SWIP and SWIS boards. The SWIP is the parallel interface to the system, which attaches directly to the NCU on the backplane. The SWIS is a serial interface used for communication with the power subsystem and attaches to the central cabinet distribution board.

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To verify connection for the parallel cable, it should be noted that a jumper exists between pins 1 and 100 on the backplane. If the cable is installed correctly the resistance between these two pins should measure as a short. Pin 1 on the connector is the upper left pin of the connector and pin 100 is in the lower right position.

There is a new display used with the OPUS that can come in handy. This command is "dump_swip". When entered, this will display the contents of various registers on the SWIP as follow:

swip_bsrc_msb:	16*10
swip_bsrc_lsb:	16*10
swip_force_par_err:	16*00
swip_misc:	16*80
swip_int_level_ctl:	16*90
swip_int_ena:	16*40
swip_int_stat:	16*00
swip_force_int:	16*00

The contents of these registers should appear as above. If they have other bits set, it is possible that the system will be unable to boot and generate a "NCU Bus Error". If this occurs it will be necessary to manipulate the registers to the values shown above. For example:

put swip_force_par_err 16*00

If the register does not change run "cleanup" and reissue the put command.

This process can be followed for any register shown above.

Al,

3.5.11 C3800 Firmware Update Procedures:

In order to install and execute new firmware for the power subsystem, it is necessary to install the new firmware and make the master changes in the file "/diag/db/fw_rev_update, which appears as follows:

.....continued on next page.....

'/diag/bin/cdb_update bpc_master_fw_rev "2.13"
'/diag/bin/cdb_update enforce_fw_revs 0';;
'/diag/bin/cdb_update bpc_master_fw_rev "3.13"
'/diag/bin/cdb_update enforce_fw_revs 1';;
'/diag/bin/cdb_update ppc_master_fw_rev "2.4"

After making the ppc or bpc master entry necessary then the script should be executed. This will update the cdb file.

To upgrade the ucode the process is similar. Make the appropriate entry in the file "/diag/db/ucode_rev_update" and execute it. This file appears as follows:

/diag/bin/cdb_update master_sr_rev 1.15
/diag/bin/cdb_update master_us_rev 4.78
/diag/bin/cdb_update master_ua_rev 1.2
/diag/bin/cdb_update master_ul_rev 1.1
/diag/bin/cdb_update master_vd_rev 1.2

It should be understood that changes made directly to the cdb file, using cdb_update, or cdb_browser will not be permanent.

Al,

3.5.12 C3800 Voltage Margins

It is possible to margin voltages on a C3800 in the following format:

altsetpts -vee10k -5.304 sp0 sp1
altsetpts -vee -4.590 sp0 sp1
altsetpts -vtt -2.04 sp0 sp1
altsetpts -vttga -2.04 sp0 vp0

The utility "altsetpts" is only temporary and when the system is rebooted, the voltages will return to their preset values. However, "altsetpts" is the only means to margin voltages on individual boards.

The permanent means of margining voltages is as follows:

.....continued on next page.....

1) edit the file /diag/db/lab_machine from a 0 to a 1

   file appears as "/diag/bin/cdb_update lab_machine 0"
                                                ^ change to 1

2) Edit file /diag/db/set_lab_busses, changing voltages to desired values. There are several categories of voltages in this file and care should be taken to avoid changing any other except those voltages listed under lab values.

   This file will appear as follows:

```
#set nominal values for lab machines (When lab_machine 1)
#lab values
vcc="5"
vee="-4.5"
vtt="-2"
vttia="-1.905"
vttsp="-1.905"
vttvp="-1.905"
vttcu="-1.905"

vttga="-2"
vttgaia="-2.07"
vttgasp="-2.07"
vttgavp="-2.07"
vttgacu="-2.095"

vee10k="-5.2"
m5v="-5"
xvee="-4.5"
xvtt="-1.905"
xvttga="-2.1"
ppcvcc="5"
ppcm5v="-5"
```

.....continued on next page....

```
#production values (These are used when lab_machine is set to 0)
vcc_p="5"
vee_p="-4.5"
vtt_p="-2"
vttga_p="-2"
vee10k_p="-5.2"
m5v_p="-5"
xvee_p="-4.5"
xvtt_p="-2"
xvttga_p="-2"
ppcvcc_p="5"
ppcm5v_p="-5"
```

NOTE* It should be understood that no margins should be changed in this file unless instructed to do so. It should also be understood that when changing one voltage value, all others must be moved to nominal, or problems will result.

Al,

3.5.13 C3400 1115 Read Data Bus Parity Error Hard Errors

A problem has been found in the C3400 that can cause 1115 Read Data Bus Parity Error hard errors. This error will happen when using the debugger and you encounter an instruction that causes an arithmetic fault. The following hard error display is the signature of the 1115 hard error caused by the debugger.

```
[SPU @11:13:16] hard_logger:revision 1.0 (Mon Nov 11 09:16:53 1991)
CPU0/JCPU: Hard error detected.
CPU0/JCPU: [#1115] se[]: read data bus parity error
CPU0/JCPU:     se[0].q5_rdata_pe - both lsw and msw parity errors
CPU0/JCPU:     se[1].q5_rdata_pe - both lsw and msw parity errors
CPU0/JCPU:     field               se[0]       se[1]
CPU0/JCPU:     se[].q5_rdata_pe:   0x00000003  0x00000003 ( 2 bits)
CPU0/JCPU:     se[].q5_bkdr_rsrc: 0x00000000  0x00000000 ( 3 bits)
CPU0/JCPU:     se[].q5_addr:       0xa0000023  0xa0000023 (32 bits)
CPU0/JCPU:     se[].q5_reqource:   0x0000000a  0x0000000a ( 4 bits)
CPU0/JCPU:     se[].rdata_pe_out: 0x00000001  0x00000001 ( 1 bits)
CPU0/JCPU:     se[].q5_rpar:       0x00000000  0x00000000 ( 8 bits)
CPU0/JCPU:     se[].q5_rdatau:     0x00000000  0x00000000 (32 bits)
CPU0/JCPU:     se[].q5_rdatal:     0x00000000  0x00000000 (32 bits)
```

```
CPU2/JCPU: hard_err is not set
CPU4/JCPU: hard_err is not set
CPU6/JCPU: hard_err is not set
```

Note that both se[0] and se[1] columns are the same and that the lines se[].q5_rpar, se[].q5_rdatau, and se[].q5_dratal fields are all zero.

Any signature other than the one above is not caused by the debugger.

This problem has been corrected in microcode, and will be included with the next release of the diagnostic database for the C3400 in the near future. If you have a customer that must use the debugger before the new microcode is available, please contact me.

Dave Muir

3.6.1 C3800 Debug Scripts

There are several scripts located in the /diag/hw directory that are used in the factory to debug failures. Most of these will not be of value to the field as there are diagnostics available that will accomplish what is needed. For some failures though, use of the following scripts may help confirm a defective board.

1. NCU Failures:

Located in /diag/hw/cutest, these scripts test the NCU intensively. These scripts can be run individually by entering the script name (i.e., ncutestC0 would test only the Read/Write registers) or all scripts can be activated with the ncutestall command.

A Series - READ/WRITE OF COMMUNICATION REGISTER SPACE i
ncutestA0 - Simple write/read of one two addresses -- check identity
ncutestA1 - Test Longword vs Word accesses
ncutestA2 - Read-after-write tests
ncutestA3 - Increment Tests
ncutestA4 - RDCMR WRCMR
ncutestA5 - TST LCK ULK PUT_S

B Series - ASAP STATE FILE AND LOOKUP
ncutestB0 - ASAP lookup and priority rotation
ncutestB1 - Read/Write of TAM and Forkposted regs, testing locks and state file.
ncutestB2 - CPU mask test ncutestB3 - Rdcmr/wrcmr test

C Series - IO SPACE
ncutestC0 - Read/write all regs
ncutestC1 - Read/write lock bits/ION, Read-after-write and WD/LW access tests
ncutestC2 - CMR/IO separtion

D Series - TRAP DISPATCH AND INTERRUPT
ncutestD0 - Basic CPU Interrupt Dispatch
ncutestD0a - Broadcast vs Non-broadcast test and Idles
ncutestD0b - Local Enable test
ncutestD0c - Global Enable Test
ncutestD0d - Test all channels
ncutestD1 - Deadlock Traps
ncutestD1a - Deadlock Trap installed XECN test (XECN aborts false deadlocks)
ncutestD2 - Firmware Traps

.....continued on next page.....

ncutestD3 - ITC Interrupts
ncutestD4 - Lock conditions of Trap Command Register
ncutestD5 - DSI and ENI effects on Traps
ncutestE0 - TOC Holdoff test
ncutestE1 - ITC holdoff test

ncutestall - to run all the tests.

usec_check - Checks that the usec enable is getting from the NCU to the NCU. It is best to run this after running ncutestE0.

2. The following scripts, located in /diag/hw, will assist you when trying to isolate C3800 memory or NIA related problems.

nmb_errs - Reports nmb detected hard or soft errors.

nmc_test - Performs connectivity tests of all testable signals between the nmb and the nmcs.

pb_walk - PBUS loopback and functional test of the NIA.

Refer to the appropriate manpage for further information concerning these three scripts.

Jerry

3.6.2 C3800 SPU Console Bug

The following statement being printed in the SPU Console window of C3800 systems is a software bug.

iobus level 7 interrupt not serviced.

This problem will be corrected in the next spu software release.

Jerry

3.6.3 Voltage/Temperature Monitoring Command in SPUOS

There is a little know command on the SPU that will provide the voltages and temperature of both MBCU's or VBCU's. This can be used for monitoring voltage changes and our temp changes. This is some of the information that is buried in EGOS. This example was done on a V9.0 Machine.

```
Usage: env -c ccu_number [-f]
  -f for forever loop (^C to abort)

# spucmd env -c -3
+ env -c -3 env: using CCU 3
VB0: +5V= 5.05 +12V=12.00 -12V=-12.10 TEMP=26.35c (79.43f)
VB1: +5V= 5.05 +12V=12.15 -12V=-12.20 TEMP=27.54c (81.57f)

# spucmd env -c -6
+ env -c -6 env: using CCU 6
MB0: +5V= 4.95 -5V=-4.95 +12V=12.00 -12V=-11.80 TEMP=27.11c (80.79f)
MB1: +5V= 5.00 -5V=-4.95 +12V=12.00 -12V=-11.85 TEMP=31.63c (88.93f)
```

Hope this helps.
Rich

3.6.4 C3000 Site Prep Guide Error

There is a error in the CONVEX I/O Site Preparation Guide, October 1991 edition, page 4-5.

The Hubble plug style for the EXP-302 cabinet is incorrect. The plug is listed as 360P62, it should be 2611, the same as the Exp-301. Please make a note of this. It will be corrected in the next release of the doc.

Thanks
Rick Pfeffer

3.6.5 ACL v1.1 s/w and Dumps

When using the U, unattended dump, option of dump the user must give enough VSNs on the tpmount(1) command line for the dump to complete. If the user does not list enough VSN's or no VSN's at all, the dump will abort while trying to use tpswitchvol(1).

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For example if you expect to 3 tapes in dumping /usr the following tpmount would be used:

unix% tpmount -t mt -m char -s DUMP_TAPE vol1,vol2,vol3 unix% dump 0GEUf DUMP_TAPE /usr

It is important to note, when using unlabeled tapes the tape daemon has no way to confirm the correct volume was mounted.

Kelvyn

3.6.6 C2xx Neutral Connection

The neutral lead has never been installed on the domestic PDU, so installation serves no purpose, except as a possible antenna.

The international systems are not affected by this.
Al,

3.6.7 C2/C3200 SCM Code Changes

In order to make the C2 (3200) more robust, over the past 18 months various changes have been made to the SCM ucode. In addition the ACPWROK line has been eliminated. These changes, combined, now allow the system to remain up after taking specific power related errors. These error, particularly, include the 8x series.

Because of this, it is not at all unusual for the system to remain up and display the error code on the front panel and illuminate the attention led.

This situation will only occur if the configuration can remain up on the remaining power supplies. So, do not be concerned if a system, particularly one with 4 memory pairs will not be sustained through a power supply failure.

This is considered a feature and should not cause any problems, except that you will have some time to replace the failed supply.

Al,

3.6.8 C3800 Intermittent Failures

The following are ongoing experiments to alleviate the following known intermittent failures:

1) Purge Rams -- The attempt here is to reduce the noise level on the ref for these components by adding a capacitor. So far this has reduced the noise level from 180 mv to 50 mv.

2) NMUL -- Again Vref is being modified on both the NVP and NSP to increase the level by 40 mv.

3) NVRF -- This is virtually the same solution as that for the purge rams.

4) SP to VP failures (NIS)- The attempt here is to reduce the noise between these two boards, by margining VTT and VTTGA. Currently VTTGA is being set to -2.05 and VTT is set to -1.95.

These are not, yet, definite solutions to these problems, but they do seem improve the system performance in these areas.

In addition, it has been determined that they are effective enough to begin upgrading systems and install these fixes on new builds.

Al,

3.6.9 Displaying The C3800 System Serial Number

To display the system serial number on a C3800 it is only necessary to perform the following:

```
get mach_serial_number
```

This will then return with a hexadecimal display of the serial number. The value will appear as a0xx.

Al,

3.6.10 Setting up the OPUS Modem

This is the procedure for getting the modem functional on the OPUS. This should not be necessary as all should be done in the software, but in case a more indepth explanation is necessary.

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Each time the rc.local script is run, the modem is initialized with the command '/diag/bin/modem_-init'. All this does is open the modem tty, and send several AT commands to it. The commands that it sends are simply listed in the text file "/diag/db/modem_parms". If the modem is not the FasTalk, some of these commands may need to change. There are three settings that are important.

The modem needs to be in auto-answer. On the FasTalk this was accomplished with a "ats0=1"

The modem needs to talk to the tty at 9600 baud, regardless of the connect speed (this is usually the default). This had to be set on the FasTalk because its default was a thing called 9600 trellis mode, which does not work well with any modem other than a FasTalk. On a FasTalk the command that does this is "at%b9600".

The modem needs to use the carrier detect line. Most modems have this defaulted to turn the line on and leave it on - if that is the case, getty will grab the tty line and try to talk to it (forever). This causes logins to constantly time out, and you won't be able to dial out. The command that does this on the FasTalk was "at&c1".

It is also noted that the operating mode is set to Normal, this turns off error correction. This is not desirable, but at any rate "at\n0" is the command to enable this.

Al,

3.6.11 OPUS Screen Characteristics and Network Use

As follow are the characteristics of the Opus screens, on the C3800, and the functionality of using them on a network:

The xsfp is the program with the representation of the keyswitch. It does a lot of little things; it provides buttons for booting, a toggle for the printer, and a radio box for the boot mode. But its main job is to provide SPU security. It restricts workstation keyboard and mouse IO when the keyswitch is in the SECURE position. For this reason, if it goes away, so does X. It is this feature that makes the xsfp non-restartable.

The xsfp receives interrupts from the hardware whenever the state of the keyswitch changes. It uses this information to determine when to boot OS, and when to restrict user input. These interrupts are only sent to one process at a time. For this reason, there can only be one xsfp running at a time.

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The CONVEXOS CONSOLE is the window that CONVEXOS should always be booted from. It is basically an xterm, but has added features that make it unique. It provides the functionality to dump characters written to the screen to a printer. The CONVEXOS CONSOLE also allows a user, logged in as rmtdiag, to take control of the window from a remote tty. This is explained in greater detail below.

If destroyed, CONVEXOS CONSOLE is restarted automatically by the xsfp. This is fine as long as CONVEXOS is not booted. The problem when CONVEXOS CONSOLE is booted is that the console driver is no longer associated with the window, and since the console driver is not restartable, the system enters a state of limbo. I would expect that any program running on CONVEXOS that would cause the console driver to write, would hang. Much the same affect as doing a control S on a C2 spu terminal. The moral of the story is never kill a window that has CONVEXOS booted in it.

The other window of importance is the SPU CONSOLE. There is absolutely nothing special about this window. It is an xterm that is given the -C flag. This simply means that messages written to /dev/console from programs running on the SPU workstation will appear in this window. Note that this window only displays the /dev/console messages until another xterm is started with a -C option. This can potentially lead to confusion.

But this is supposed to be about remote control of the CONVEX. There are two levels of remote interaction, one is simple, providing access to the CONVEXOS CONSOLE window, the other has a bit more complexity but offers complete control of the SPU from a networked workstation running X.

rmtdiag

To gain control of the CONVEXOS CONSOLE window, one simply logs in as the user rmtdiag. When this user logs in, the CONVEXOS CONSOLE is told which device rmtdiag has logged in through. The log in can be either through a tty port, or from an 'login'. After resizing the CONVEXOS CONSOLE window to match that of rmtdiag's terminal (resizing only works if rmtdiag logs in from a vt100 type terminal or an xterm), CONVEXOS CONSOLE begins communication with that device, and ignores keyboard input from the SPU workstation keyboard. Both the remote screen and the CONVEXOS CONSOLE recieve the same output. Since this is the window that CONVEXOS console driver runs in, the familiar ^P, ^D functionality works to give access to CONVEXOS, or the SPU.

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When the rmtdiag user is done, he cannot simply log out, since he is actually borrowing control of the window that CONVEXOS is booted in. The only "good" way to give up control is to run "remote_disconnect". This notifies CONVEXOS CONSOLE that rmtdiag is done, CONVEXOS CONSOLE quits communicating with the remote port, and again takes input from the SPU workstation keyboard.

Networked SPU

To gain broader control of the SPU, a networked SPU is used. In this case, the same programs are run on the SPU workstation, but their output is displayed on a remote workstation attached by ethernet. This is all accomplished by setting the DISPLAY environment variable in the startup script.

To make the changes, you must have root access.

In diaguser's home directory, the .xinitrc file should be modified in the following manner:

```
mwm &
xsetroot -solid navy
sleep 5 # gotta wait so that mwm gets straight before starting clients
.
.
.
becomes
.
.
.
mwm &
xsetroot -solid navy
DISPLAY=other_workstation_name:0.0
mwm &
xsetroot -solid navy
sleep 5 # gotta wait so that mwm gets straight before starting clients
```

Everything started after the resetting of DISPLAY, appears on the networked workstation. Note that the starting of the second mwm is optional, depending on whether the root display menus provided by the motif window manager are desired on the networked workstation. If the motif window manager is to be started from the SPU workstation, the networked workstation should be running an X server, but not a window manager. Conversely, if the second mwm command is omitted from the above file, the networked workstation should be running both an X server and a window manager.

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If it is desired that the SPU CONSOLE window be displayed on the networked workstation, a similar change is needed to /etc/spu_console_start. Remember that this window displays all messages written to /dev/console by programs running on the SPU workstation.

/bin/su diaguser -c '/usr/bin/X11/xterm -C -ls -name "SPU CONSOLE" -sl 500 -sb -geometry 80x23+0+0 -display unix:0.0'

.

.

.

becomes

.

.

.

/bin/su diaguser -c '/usr/bin/X11/xterm -C -ls -name "SPU CONSOLE" -sl 500 -sb -geometry 80x23+0+0 -display other_workstation_name:0.0'

Extreme care should be exercised when making this change, only the line shown should be changed.

Once this change is made, simply kill the current SPU CONSOLE window, 'init' will automatically start a replacement with the new display environment variable. Be careful when starting new SPU CONSOLES by hand. Only the "last" xterm started with the -C option will receive console output, confusion will reign if a SPU CONSOLE is started on one display when a SPU CONSOLE window is running on another (the old one simply acts like an xterm).

Additionally, the DISPLAY environment variable is set to unix:0.0 in diaguser's .profile and .cshrc files. These should also be set to identify the workstation that is to provide X services.

Thanks to Louis VanHouten for this information.

Al,

3.6.1 C3400 Series JSM Error Codes

JSM Error and Message Codes
firmware revision 1.7

Code	Error/Message
00	Deadman timer indicates JSM internal problem
02	SP-SM.PWRINTAK* failure
04	SP-SM.SMBDATA<7..0>* failure
07	SP-SM.SPUDCOK failure
08	A/D Convertor Timed Out
0B	SP4 Illegal Instruction
0D	SP4 instruction cycle timed out
0F	Checksum failure on JSM
15	CPU3 installed incorrectly
1A	CPU6 installed incorrectly
1B	CPU2 installed incorrectly
1C	SP4 installed incorrectly
1D	CUJ installed incorrectly
1E	ME0 installed incorrectly
1F	MO0 installed incorrectly
20	ME1 installed incorrectly
21	MO1 installed incorrectly
22	ME2 installed incorrectly
23	MO2 installed incorrectly
24	ME3 installed incorrectly
25	MO3 installed incorrectly
27	CPU1 installed incorrectly
28	CPU5 installed incorrectly
2D	CPU0 installed incorrectly
2E	CPU4 installed incorrectly
33	PIX installed incorrectly
34	PIY installed incorrectly

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Code	Error/Message
42	PS2 power supply temp failure
43	PS3 power supply temp failure
44	PS4 power supply temp failure
45	PS5 power supply temp failure
46	PS6 power supply temp failure
47	PS7 power supply temp failure
48	PS8 power supply temp failure
61	PS1 AC power failure
62	PS2 AC power failure
63	PS3 AC power failure
64	PS4 AC power failure
65	PS5 AC power failure
66	PS6 AC power failure
67	PS7 AC power failure
68	PS8 AC power failure
69	HMU PS5 AC power failure (-4.5V)
6A	HMU PS6 AC power failure (+5V)
6B	HMU PS7 AC power failure (-2V)
71	+5.0V DC power supply failure
72	+12.0V DC power supply failure
73	-12.0V DC power supply failure
74	-5.0V DC power supply failure
75	-4.5V DC power supply failure
76	-2.0V DC power supply failure
77	-5.2V DC power supply failure
78	HMU +5.0V DC power supply failure
79	HMU -4.5V DC power supply failure
7A	HMU -2.0V DC power supply failure
82	PS2 current sharing failure
83	PS3 current sharing failure
84	PS4 current sharing failure
85	PS5 current sharing failure
86	PS6 current sharing failure
87	PS7 current sharing failure
88	PS8 current sharing failure

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Code	Error/Message
91	-4.5V current sharing out of tolerance
92	-2V current sharing out of tolerance
93	+5V current sharing out of tolerance
A0	Intake thermistor exceeds tolerance
A1	Exhaust thermistor exceeds tolerance
A2	PI2 terminator thermistor exceeds tolerance
A3	JSM thermistor exceeds tolerance
B1	CUJ airflow failure
B2	PIY airflow failure
B3	VME airflow failure
C0	Insufficient power supplies for configuration
E0	FN0 failure
E1	FN1 failure
E2	FN2 failure
E3	FN3 failure
E4	FN4 failure
E5	FN5 failure
E6	FN6 failure
E7	FN7 failure

3.7.2 Removing OPUS Printer Cable

It is important to understand that the console printer on the Opus is connected via the swis. Removal and replacement of the printer cable should be avoided with power applied, as this can cause damage to the swis board.

Al,

3.7.3 swis Failure Indications

The indications of a swis failure can be very misleading. When the swis loses contact with the key switch on the 3800, all screens will hang along with the mouse cursor.

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When attempting to reboot the ConvexOS and xsfp screens must get a status from the key, through the swis. If this does not occur then the ConvexOS and xsfp screens can not be raised. This will force the other spu and console screens to fail, as well and abort the boot to the OPUS single user mode.

To verify that the swis is the problem it is necessary to edit the file /users/diaguser/.xinitrc (/.xinitrc). In this file place a "sleep 1000" entry as the next to last line in the file and reboot. This will allow the SPU window to stay up while troubleshooting is accomplished. The last line in the file will be "/diag/bin/xsfp -geometry +0+1000 > /dev/console 2>&1. This is the entry to bring the console window up. The sleep entry will be placed just prior to this entry.

If the swis is defective then a "dump_swis" command will generate errors. In addition any commands issued under pwr_util will hang.

Al

3.7.4 C3800 osc_freq and Released NCU's

As mentioned in a previous tech bulletin, when upgrading software the osc_freq will be reset to a 0 which is 18ns on the systems currently in the field. This will remain the case for these systems, until the NCU's fail and are replaced with released NCU's.

For released NCU's, the osc_freq = 0 will be at 16.67.

The difference between the two NCU's, is that the existing field NCU's have clocks of 16.67, 18 and 20ns. The released versions which will be a rev A will have clocks of 15.5, 16.67 and 18ns. So with the released versions and osc_freq of 0 will be 16.67ns.

All NCU's shipped from Dallas, from this point, will be rev A NCU's and not the prereleased or xecn 15 version. This can be verified with a cop.

Unfortunately for all sites currently installed, this will remain a problem until the NCU is replaced.

Al,

3.7.5 C3800 STRAMS

The STRAMS used on the C3800 refer to (Self Timed Rams). They are called this because the components require no external clocks, as standard DRAMs do. This is beneficial because it allows these components to be fully scannable.

The STRAM's are used in all caches contained on the NSP and the comm registers on the NCU.
Al,

3.7.6 C3800 Software Tapes on OPUS

The following is a list of the software and briefly how the tapes are used on the 3800 spu (Opus).
****
760-004315-000 SpuOS X1.0.0.1 (C3800 OPUS)
This tape is to be used only when a disk dies or a virgin Opus disk is being installed, it is a boot tape, not an installsw tape. All Opus OS upgrades are included in the Diagnostic Tape.
****
760-003615-00X 3800 SYS DIAG X1.0.0.5
(TAC) This is the latest Diagnostic tape and it includes the upgrade required to the Opus OS, including swip and swis code.

The scheduled release for V1.0 Diagnostics is the end of February.
****
710-010915-005 ConvexOS V10.0.2 (C3800 OPUS)
This is the latest released OS, V10.0.3 is coming very soon.

Rich

3.7.7 ConvexOS V10.0.3 Information

ConvexOS V10.0.3 is a replacement kernel for all preceding 10.0 versions of ConvexOS. It is a cumulative patch, so it includes all that was in V10.0, V10.0.1, and V10.0.2.

This patch release was necessary to fix a bug in the VVM driver, in which the driver would not fully save the state of the vector registers when "borrowing" them for the parity calculation. This problem was especially apparent on C3800 machines.

Rich

3.8.1 Multiple Screens on the Opus Workstation

It is not possible to start a second xsfp screen on the opus as this screen is hard coded to respond to certain interrupts. When a second xsfp is initiated this will force a conflict between the two screens and cause the workstation to crash. Although this will not directly crash the C3800, when the workstation is rebooted, the swis will force a reset of the power subsystem and this will bring the system down.

It is possible to startup a second ConvexOS screen, but it is unadvisable, as the two screens will compete for interrupts. This could lead to chaos as processes would be handled across both screens, making it very difficult to keep a coherent process going. The second screen, should it be necessary, can be started by entering "CONVEXOS_CONSOLE" in any window. Again, it is not recommended, except in an emergency.

Al,

3.8.2 C3800 Board Damage During Shipping

We have, recently, experienced some minor damage to C3800 boards being returned. The damage has been minimal, but usually involves some minor buckling of the frame. We believe that the cause of this is elevating the power pallet to the top.

To avoid this, stickers will be applied to the outside of the box indicating "This Side Up". In addition it is asked that board be placed in the box so that the power pallet is always at the end of the box where the wheels would mount. This is easy to determine as there is a small cutout at the opposite end where the silver handle on the board is meant to rest.

This cutout is larger than the handle in order to accommodate left and right hand boards. Please make certain that the handle fits into this cutout. This may involve turning the board over.

It is also requested that the boards be returned, packaged exactly as they are received on site.

Following these few suggestions will reduce possible damage to the boards and aid in turn around time to the field.

Al,

3.8.3 SST v2.2 Problem

The version of sst v2.2 has a problem, in that it is not possible to read the sst data patterns off of the tape. It is possible to load the tape with an installsw, but when attempting to pack the files that operation will abort,indicating that the first file on the tape is unreadable.

This problem is corrected by sst v2.2.1 and can be ordered at any time.

Al,

3.8.4 C3800 Continuity List and Functions

The following is a list of continuity and their function for the C3800:

1) sys_con -- This utility is to test for stuck at faults between the crossbar, NCU and NIA. There is, also, a limited amount signal line short testing, using the patterns 0, F, A and 5.

2) xc_con -- This utility is used to test continuity of data lines between the crossbar and NSP's, NCU and NIA. This utility is not executable, except in its home directory. Which is /diag/hw/cutest. If run with no arguments will only execute on the NCU.

   It can be run on the other devices by using the following switches: p0-p7 (for NSP head#) and i8 (for NIA).

3) xbinteg -- This is a more robust version of sys_con. It is implemented by entering xbinteg e, or xbinteg o. This will execute the test on either the odd side, or the even side of the crossbar.

4) idc_con -- This verifies continuity of the Pbus between the individual IDC and the NIA. Will use bit by bit transfers of data to memory through the NIA. Executes the following subtests:

   a) idc_init
   b) setup_piga
   c) idc_to_mem_test
   d) idc_to_nia_test
   e) idc_interrupt_test.

   Executed with idc_con <ccu#>

.....continued on next page.....

5) pb_walk -- This is a Pbus loopback and functional test of the NIA. It tests continuity as idc_con, plus the Pbus state machines. In addition this utility tests all CCU's and is not restricted. The first 3 subtests are executed on all CCU's simultaneously and the 4th is executed sequentially.

   The subtests are as follow:

   a) loopback
   b) pbi_test_NOP
   c) pbi_test_WRITE
   d) mbp_test

These are all scan based tests and included as modules of SST.

Al,

3.8.5 HSP Troubleshooting and Parts Information

This is everything that you ever wanted to know about the HSP/HIA subsystem. It is a composite of past Technical Bulletins with additional information.

1) 95% of all HSP failures will be caused by cables, or cable configurations.

2) Any failure of class 4 of the diagnostic should be approached as a cable failure initially.

3) In situations where a short set of cables run fine, but the maximum 100' set will fail class 4 of the diags, this can be caused by shorted pins on the backplane, or the adapters. This is true because the HSP link to the HIA is differential, so there may be enough current to drive a short distance, but not enough to drive the 100'.

4) Verify that the proper power supply is installed in the system. The HSP draws more current on -5 VDC. More information on the power supply can be obtained from week 29's tech bulletin.

5) For long cable runs where the HIA is in a different room from the system, the grounds, particularly AC can be a problem, as the two may be on different power systems.

.....continued on next page.....

6) Customer designed boards should not be used to troubleshoot with, as timing problems could create problems for class 4 of the diagnostics. Instead the far side echo boards should be used for this effort.

   The part number for these boards are:

   a) Control card 410-001141-200; to be installed in slot 5 of HIA
   b) Buffer card 410-001142-200; to be installed in slot 4
   c) 2 foreplane connectors 410-000106-200 (each)

7) Manuals should be obtained before working on this subsystem. The part numbers follow:

   a) Farside Echo Test Procedure 900-000299-000
   b) HSP Users Guide 081-000110-000
   c) HIA Users Guide 081-000111-000

8) HSP is a standard product and is no longer supported by Special Systems. All requests for assistance, for this product, should be directed to the TAC.

For HSP's to be installed in C2's, a multi volt power supply upgrade is required. This is because the HSP/HIA combination draws more current from -5 VDC than the standard I/O subsystem draws.

The upgrade consists of replacing the -5 VDC supply with a -12 VDC supply and adjusting it to -5VDC. This provides the necessary additional current.

There is a kit provided for this upgrade, which includes the power supply and the necessary wire harness. This wire harness will add a parallel set of wires for the -5 VDC to handle the additional current load. This harness will be required for any C2 below serial number 8420. Above this, the additional wiring is standard and will only require the power supply. To verify if this harness is necessary, check the -5 VDC post at location U80 in the lower left corner of the backplane. If 2 orange wires are not run to this point, then wire harness will be required.

NOTE Although all newer systems will ship with the cable harness installed the extra power supply will not be installed, unless the system ships with HSP installed. Anytime the HSP is added in the field a power supply will be necessary. Even on a system shipped with HSP installed, i t would be advisable to verify that the power supply is installed.

.....continued on next page.....

The part number for this kit is 550-000239-299 and the part number for the wire harness is 603-160004-200. The power supply includes a DC-DC converter.

Address space for HIA begins at C00000. The address C0000e is the address of the register on the FSE.

In addition the ioconfig entries for HSP are as follow:

hsp #
  drvr HEC-001 csr 0x00
  chnl 0-15
  type HED-001

NOTE These are standard entries when echo boards are installed. If no customer device is installed and echo boards are removed, then there should be no entry except hsp #.

If this standard entry is made and the echo boards are removed, system will encounter kerntrap vector 2's when autoconfig is run. This will not halt booting.

A problem exists with the hsp adapter cable between the backplane and the cable to the HIA (p/n 601-600012-200). The problem is that the cable is not trimmed close enough at the connector. The symptoms are failure of class 2 subtests of dev4120, particularly subtest 241.

The solution is to trim the cable.

This is the only known diagnostic failure for the HSP.

Almost all HSP failures have been found to be cable related. So this should always be the first thought when troubleshooting in this subsystem. For diagnostic failures at subtest 4200 and above, the 3 HSP/HIA cables are nearly always the problem.

Al,

3.8.6 C3800 Power Brick Locations

The following will indicate locations of the power bricks located on the power pallets of C3800 boards. All locations are slightly skewed for each board, so each board will be displayed separately.

.....continued on next page.....

NOTE When replacing a power brick, it is recommended that the accompanying fuse be replaced and vice versa.

All displays from heat sink side left facing as viewed from heatsink side.

N C U P P

SPARE VEE -4.5 F S6	SPARE VTT -2 E S7	VEE -4.5 E S8	VEE -4.5 D S9	VEE -4.5 C S10
VTT -2 B S1	VTT -2 C S2	VTT -2 D S3	VEE -4.5 B S4	VEE_IOK-5.2 A M5
VTT_GA -2 A M1	VTT -2 A M2	VCC +5 A M3	VEE -4.5 A M4	

.....continued on next page.....

N V P P P

VTT_GA -2 H S6	VTT -2 C S7	VEE -4.5 B S8	VTT -2 D S9	VTT_GA -2 C S10
VTT_GA -2 B S1	VTT_GA -2 C S2	VTT -2 B S3	VTT_GA -2 E S4	VTT_GA -2 F S5
VTT_GA -2 A M1	VTT -2 A M2	VTT_GA -2 D S13	VEE -4.5 A M4	

.....continued on next page.....

N S P P P

VTT_GA -2 F S10	VTT -2 D S9	VEE_IOK-5.2 B S8	VTT -2 C S7	VTT_GA -2 G S6
VEE_IOK-5.2 A M5	VTT_GA -2 E S4	VTT -2 B S3	VTT_GA -2 C S2	VTT_GA -2 B S1
	VEE -4.5 A M4	VTT_GA -2 D S13	VTT -2 A M2	VTT_GA -2 A M1

.....continued on next page.....

N M B P P

VEE -4.5 D S10	VTT -2 E S9	VCC +5 B S8	VTT_GA -2 B S7	VCC +5 C S6
VEE -4.5 C S5	VEE -4.5 B S4	VTT -2 D S3	VTT -2 C S2	VTT -2 B S1
	VEE -4.5 A M4	VCC +5 A M3	VTT -2 A M2	VTT_GA -2 A M1

.....continued on next page.....

C C U P P

VCC +5 D S10	VCC +5 E S9	VCC +5 F S8	VCC +5 G S7	VCC +5 H S6
VEE -4.5 B S5	VEE -4.5 C S4	VEE -4.5 D S3	VCC +5 B S2	VCC +5 C S1
	VEE -4.5 A M4	VCC +5 A M3	VTT -2 A M2	-5VDC -5 A M1

.....continued on next page.....

N I A P P

VTT -2 D S10	VEE -4.5 C S9	VEE -4.5 D S8	VTT -2 E S7	VEE -4.5 E S6
VEE_IOK-5.2 A M5	VEE -4.5 B S4	VTT -2 C S3	VTT -2 B S2	VTT_GA -2 B S1
	VEE -4.5 A M4	VCC +5 A M3	VTT -2 A M2	VTT_GA -2 A M1

Al,

3.8.7 C3800 Memory Soft Error tools

There are two tools that can be used to isolate memory soft errors. These are "dump_soft_log" and "mam". The "dump_soft_log" tool will allow you to retrieve soft errors that have occurred on the system but as it has a couple of bugs you must also use "mam" to isolate the nmc actually reporting the error. The following are examples of how to use these two tools.

spu> dump_soft_log

```
      LOG STARTED: Jan 00 00:00 1900
   TOTAL FAILURES: 21
   FAILED DEVICES: 13
ERRORS NOT LOGGED: 0

             B S
 M           I T
 B  DEVICE   T K   FIRST FAIL          LAST FAIL       ADDR    #FAILS
-- -------- -- - ---------------   ---------------- -------- ------
LATEST FAILURE:
1e  Z032A4   20 0 Feb 05 06:48 1992 Feb 13 07:44 1992 1eec9ef8 000002

EARLIEST FAILURE:
0e  U002B1   29 0 Jan 11 00:46 1992 Jan 20 02:56 1992 003de868 000006

LOGGED FAILURES:
0e  U002B1  29 0 Jan 11 00:46 1992 Jan 20 02:56 1992 003de868 000006
1e  Z032A4  20 0 Feb 05 06:48 1992 Feb 13 07:44 1992 1eec9ef8 000002
```

You must then use the "mam" tool to identify the nmc. Example:

---

spu> mam 4 1eec9ef8

```
EVEN REQUEST
Board 16#1
Bank  16#f
Row   16#3
row_add 16#6a6
col_add 16#7d6
```

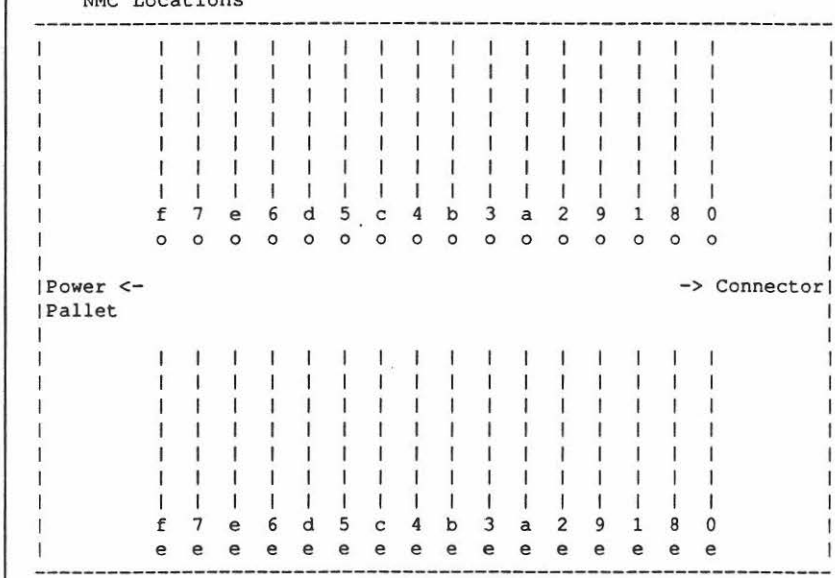
.....continued on next page.....

The failing nmc for this entry is fe on nmb1.

The following is an explanation of the above "mam 4 1eec93f8" entry.

```
mam = script name
4 = number of memory boards in the system.
1eec93f8 = the physical address taken from the ADDR column of the
           dump_soft_log print out.
```

To identify which nmc to remove (in this example fe), use the following chart.



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The "mam" tool may also be used to isolate ecc errors. As the ecc errors are not recorded in the /mnt/errlog, the only time you will be able to retrieve this information is when you actually see the error being reported on the console screen or after OS is shutdown, you can utilize the "nmb_err" tool (see the manpage for nmb_err) to obtain the address location. DO NOT USE THE "NMB_ERR" TOOL WHILE OS IS ACTIVE AS THIS WILL CRASH THE SYSTEM.

Jerry

3.9.1 C3800 PPC Brick Fuses

There are two fuses associated with each power brick on each ppc. These are 1/2 amp and 3 amp fuses. The resistance of each fuse, cold out of the circuit, measures:

1/2 amp = 1.65 ohm 3 amp = .071 ohm

Jerry

3.9.2 C3800 Opus Thermal Problems

It is possible for the OPUS workstation on the C3800 to exhibit some heat related failures upon initial bowered. These thermal problems exhibit themselves as diaginit failures. Specifically the system will fail to scan and hang, or fail while running spu4000 subtests 411 and 412 during diaginit.

The problem is caused by the drivers on the swip getting too hot on initial boot of the OPUS.

The temporary workaround is to remove the SWIP to NCU cable, at the NCU, when booting the OPUS after experiencing this failure. So far this symptom has not been experienced in the field because the workstations are left alone most of the time. But, it is possible to experience the failure anytime the OPUS is rebooted.

The problem does not occur during normal operation.

Jerry

3.9.3 C3400 Hard Error 1120 - External pte Tag Parity Error

If you see one of these errors on a C3400, it may be a soft error in the purge ram.

```
CPU2/JCPU: Hard error detected.
CPU2/JCPU: [#1120] external pte tag parity error
CPU2/JCPU:  field                  se[0]       se[1]
CPU2/JCPU:  se[].epte_tag_pe_out: 0x00000001  0x00000001 ( 1 bits)
CPU2/JCPU:  se[].q5_tagp:         0x00000000  0x00000000 ( 1 bits)
CPU2/JCPU:  se[].q5_tag:          0x001c3200  0x001c3200 (21 bits)
CPU2/JCPU:  se[].q5_addr:         0x0017b000  0x0017b000 (32 bits)
```

.....continued on next page.....

Please run the following utility to determine if it a purge ram error.

(spu)> pte_cache -c (cpu number) (se[].q5_addr)

example:
pte_cache -c 2 0017b000

pte_cahce: revision 1.0 (Mon Nov 11 09:16:53 1991)
Dumping pte_cache for cpus: 2

CPU	VIRT ADDR	PHYS ADDR	VAL	REF	MOD	CIR	TID	TAG	TAGP	RWE	TL	BYP	SW
2	007A7000	0017b000	3	2	3	0c	0c	800	0	110	0	0	000

If the VAL, REF, or MOD have a value of 1 or 2, then it is an error in the purge ram. These fields should only be 3 or 0.

The same hard error message may be caused by other problems, so it is important to know if the error in the VAL, REF, or MOD fields of the rams.

The next release of the System Diagnostics and Diagnostic Database tape will treat a purge ram error as a soft error and continue operation. The new diag and diag database should begin shipping in the near future.

Dave

3.9.4 MCM3 - Information Update

Because of a minor error in the previous release of this document, I am resending this. This document supersedes all previous versions. Please do not confuse this with previous releases. The primary difference is the location of dmm's in half populated configurations.

Like the MCM and MCM2, the failed component location can be determined from the memory address. The same basic rules apply, but is somewhat more complex because of the concept of physical and logical banks. To understand this concept, keep in mind that there are 16 physical banks on the MCM3 and it takes 2 physical banks to make up one (1) logical bank. This can be seen from the drawing and table below:

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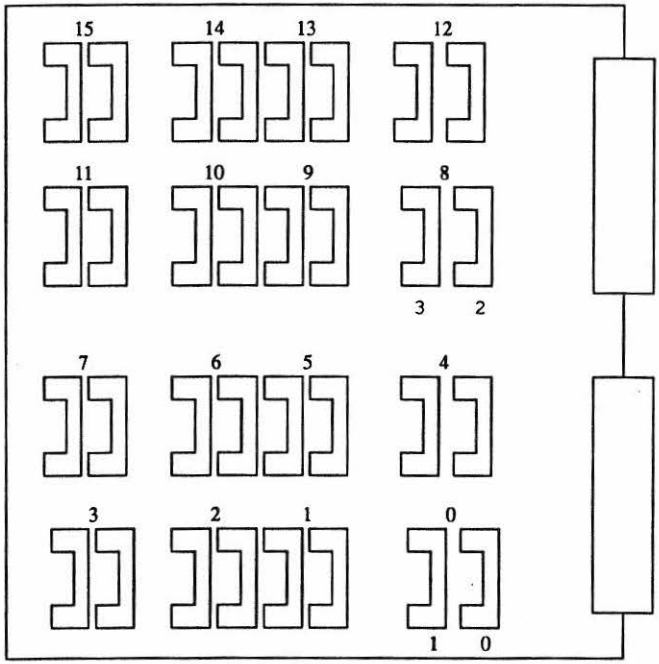
MCM3 PHYSICAL BANK LOCATIONS
(Each bank consists of 1 pair DMM's



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LOGICAL BANK	CORRESPONDING PHYSICAL BANKS
0	0,8
1	1,9
2	2,10
3	3,11
4	4,12
5	5,13
6	6,14
7	7,15

As can be seen from the table and drawing above, the physical banks that produce the actual logical bank reside on different halves of the MCM3. For example; Logical Bank is made up from physical bank 0 which is in the lower right corner of the MCM3 and physical bank 8 which is the same position on the top half of the board. It should be noticed that there are two DMM slots for each physical bank.

One other concept that is different is the fact that the MCM3 can be 1/4 or 1/2 populated. In other words you can place 8 or 16 DMM's on the board, rather than the 32 for a fully populated MCM3. To accomplish this for 1/4 populated, it is necessary to install one (1) DMM in each physical bank 0-7. In addition it is important to know that the first DMM slot is on the right, as shown in the drawing above. Note that physical bank 0 has DMM slots labeled 0 and 1.

To produce a 1/2 populated board the same rules would apply, except that one DMM would be placed at location 0 and 1 in the lower 8 physical banks.

Because the board has so many configurations the addressing is more complex than in the past. Because of this complexity, it will be necessary to give several variations on this representation.

1Mb (256kx4) DRAMS
1/4 Populated

MCM Pairs	Physical Memory 0	Pair Select	Row Select	Logical Bank	Even=0 Odd =1
1	32MB	-	28	5..3	2
2	64MB	6	28	5..3	2
4	128MB	7,6	28	5..3	2

.....continued on next page.....

1/2 Populated

		1 0			
1	64MB	-	25,24	5..3	2
2	128MB	6	25,24	5..3	2
4	256MB	7,6	25,24	5..3	2

Fully Populated

		2 1 0			
1	128MB	-	28,25,24	5..3	2
2	256MB	6	28,25,24	5..3	2
4	512MB	7,6	28,25,24	5..3	2

4MB (1Mx4) DRAMS
1/4 Populated

1	128MB	-	28	5..3	2
2	256MB	6	28	5..3	2
4	512MB	7,6	28	5..3	2

1/2 Populated

		1 0			
1	256MB	-	28,31	5..3	2 **
2	512MB	6	28,31	5..3	2 **
4	1GB	7,6	28,31	5..3	2 **

Fully Populated

		2 1 0			
1	512MB	-	29,27,26	5..3	2
2	1GB	6	28,27,26	5..3	2
4	2GB	7,6	28,27,26	5..3	2

**For 1/2 populated with 8MB DMM's bit 26 is used for row select, but if used in conjunction with MCM 2's then bit 31 is used instead of 26.

Pair Select - Board Pair experiencing problem
Row Select - Indicates binary weight of DMM location
Logical Bank- Binary weight of logical bank 0-7
Even/Odd - Indicates Even or odd board in pair

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To figure the location of the failed DMM think of the logical bank in terms of both physical banks combined. This produces DMM locations 0-3 with 2 and 3 residing in the upper physical bank. Note Drawing above for numbering of DMM locations in physical bank 0 and 8.

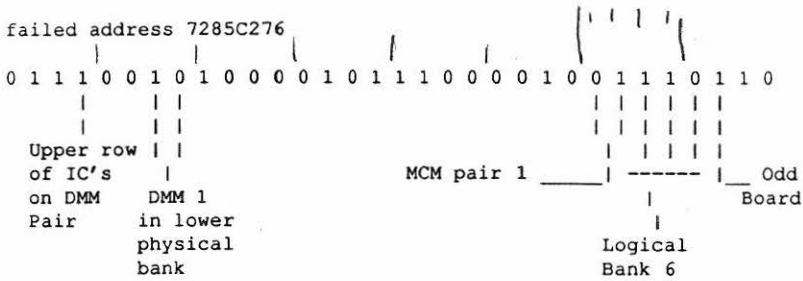
In the case of the 1/4 populated board, bit 28 just indicates the side of the DMM in error, where a 1 indicates the upper side. Keep in mind that each DMM consists of 10 DRAMs on both sides and each side is considered a row.

For the 1/2 populated board bit 24 will indicate whether the Failed part is in upper or lower physical bank and bit 25 indicates the side. For the 4MB DRAMS 28 and 26, respectively, are used for the same reference.

For fully populated boards with 1MB DRAMs bits 24 and 25 will give the location of the DMM and bit 28 will be the failed DMM row. For the 4 MB DRAMs it'll be bits 26 and 27 for the DMM slot and 28 for the DMM row.

The following example may clarify the explanation:

The example is for a system with 4 board pairs of fully populated MCM3's with 1MB DRAMs installed:



	PART NUMBER
Unpopulated MCM3	410-002230-200
2MB DMM	411-000204-200
8MB DMM	411-001204-200
2MB DMM	411-003204-200 Can only be used with MCM3 to be determined later.

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* 4MB DMM will only be manufactured if absolutely necessary.

PREREQUISITES

1) 4.1 Diagnostics
2) 4.0 Diagnostic Database
3) Diagnostic: mem4100
4) CUO 6221 and CUE 6222 for 2GB system
5) CUO 3221 and CUE 3222 for 1GB system
6) CPX 6201 for 1GB, or 2GB standard C2 system
7) PI2
   a) 1224 rev E
   b) 2224 rev H
   c) 3224 any rev
8) CPX 2201 and 4201 must be at rev M when installing 128MB or 256MB MCM3's.
9) MCM3's cannot be installed in C201's or C202's, because of timing.

The MCM3 can co-exist in the same system as either the 3213 MCM, or the MCM2. It cannot, however, be installed with the 1213 MCM's. **

**All upgrades are necessary that would be required for 3213 MCM's. (i.e. ASP rev K and SP2 rev L and PIA rev H)

The documentation for the MCM3 will be chapter 4 of the C3400 "Theory of Operation" Manual.

The iscan utilities mcm_func and mcm_scr have been modified for use with the MCM3.

Al,

3.9.5 C3800 Continuity Test After Board Replacement

It should be understood that anytime a board is replaced on installed in the C3800 that it is necessary to run the appropriate continuity tests, as it is possible that the board has not seated properly. The continuity tests necessary will normally involve spu4000 subtest 810 for memory boards and subtest 812 for NSP's and NVP's. For replaced xbar boards it is recommended that xbinteg and xc_con be used.

The discussion of the various continuity tests is detailed in tech bulletin v3w8. Please read this for further details.

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If the continuity tests are not executed, it is possible that failures in OS can be misinterpreted.

Al,

3.9.6 dev_vscsit Failure in Subtest 300

Please, be aware that the diagnostic dev_vscsit will fail subtest 300 on a new DAT tape. This is caused by a rewind timeout of insufficient duration to allow the full rewind operation and the file writing necessary on a new tape. This is only observed on new tapes and the diagnostic will run successfully on subsequent passes of the same tape.

A work around for the problem is to use the -n option when running the diagnostic. This will cause dev_vscsit to ignore the timeout.

Al,

3.9.7 C3800 display_log Utility

For situations when the cause of a system crash is very vague and not easily identified, a utility exists to display all of the console messages, and other assorted information about the system. This utility is known as the "display_log". This utility is quite helpful in isolating subtle problems with the C3800. It is particularly useful with subtle power problems that would not normally be noticed.

This utility can be entered from the spu in the form "display_log -x > file". Where x is a number, representing number of days, in a range of .1 to 5. Redirecting the output to a file is only necessary to save the contents, it could just as easily be piped to less, or more.

It is not unusual for the contents of the "display_log" to be requested by Dallas when a problem is pursued.

Al,

3.9.8 Error Dumpers Filling the Root File System

It is possible for the new error dumpers to fill up the root file system, because of the limited space available. Because of this, in future releases of the diagnostics the dump files will be moved to /sst. The new dump files include the pram.out and nvrf.out dump files.

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In the meantime the problem can be solved by moving the dumped files from /users/userdiag to /sst.

Al,

3.9.9 OPUS Workstation Crash on C3800

It has, recently, been discovered that the OPUS workstation on the C3800 is capable of crashing and indicating in the file /var/adm/messages that it failed with a memory parity error. This is caused by swip and swis address space that is currently being changed.

So any suspected memory should be confirmed before pursuing. This can be accomplished by running the memory selftest, or by waiting for the next occurrence and verifying the address is the same.

Al,

3.9.10 C3800 Crossbar Power Pallets

Be aware that there are two crossbar power pallets in the C3800. There is an even and odd side power pallet. The even side power pallet supplies power to the XCL as well as all of the even side xbar boards. In addition the power pallet controller for both power pallets, is located on the even side pallet.

In order to reduce costs, only the odd side pallet is provided as a spare. There is no problem here, as it is relatively painless to convert the odd side pallet to the even side.

To accomplish this, it is necessary to remove the mounting hardware, remove the plugs on the mounting holes on the supply and mount the new supply to the even side bracket.

It should be understood that the even side supply is under greater load, so in emergencies, it may be possible to move a weak pallet from the even side to the odd side until a replacement can be secured.

In order to verify that the even pallet may work on the odd side, it is possible to remove the XCL and power the xbar up using pwr_util. If the crossbar will power up with the XCL removed, it is a candidate to be moved to the odd side. The xbar can be powered up manually by using the k and l options of pwr_util.

If the odd pallet fails then there is little that can be done except to replace it.
Al,

3.9.11 C3800 Crashes Caused by Power Problems

It is important to understand that power problems can play a part in many hard crashes and not necessarily be very obvious. In many cases the component that reports the crash is not the one experiencing the power failure.

Quite often the failure will be lost in the noise, but upon closer examination a power problem will be found, either by examining the "display_log", or by examining the error more closely. When this happens the error will be reported, quite often, as a PPC failure. This PPC failure will be followed by a number, as

#BPC: 0 PPC: 4 Warning: 300 volts removed from pallet
#BPC config error code: 00 PWR config error code: 19

This failure indicates a problem with the power pallet on board number 4 in bay 0. To determine the correct location of the failure it is necessary to count across bay 0 to the correct board. It is important to understand the correct sequence and the fact that slots 0 and 7 will, likely, be empty. In this case the failure will be with NVP 1.

```
0 1 2 3 4 5 6 7

C N N N N N N C
C M S V V S M C
U B P P P P B U
P             P
P             P
```

In addition, the BPC status display at the time of boot, or from pwr_util can be used to isolate the failed module. In the case below, again the failure is identified as slot 4. Notice that slots 0 and 7 indicate no activity.

.....continued on next page.....

```
[K#--> Bay Power Update Returned 00 ppc mask for bpc uart 0
[K#SW Info (DiagIN236): Bay Power Controller status message
[K#
[K#PPC Status for BPC number 00
[K# bay pp fw prt bkpln bkpln plt bd bd bd bd bd bd bd bd bay bps bus bus
[K# cnf cnf rev id slot type  typ 0  1  2  3  4  5  6  7  pwr num OK  on
[K#0|ff  ff  ffff ff  ff  ff  ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
[K#1|00  00  0205 00  06  02  01 01 00 00 00 00 00 00 00  00  00  00  00
[K#2|00  00  0205 00  07  02  02 02 00 00 00 00 00 00 00  00  01  00  00
[K#3|00  00  0205 00  08  02  06 06 00 00 00 00 00 00 00  00  01  00  00
[K#4|00  00  0205 01  09  03  06 06 ff ff ff ff ff ff ff  19  02  01  ff
[K#5|00  00  0205 01  0a  03  02 02 00 00 00 00 00 00 00  00  04  00  00
[K#6|00  00  0205 01  0b  03  01 01 00 00 00 00 00 00 00  00  05  00  00
[K#7|ff  ff  ffff ff  ff  ff  ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
```

It is, also, quite common for the board reporting a hard error to have nothing at all to do with the failure. So hard errors should be examined very closely to determine their actual meaning.

Al,

3.9.12 C3800 pram.log Created by New hard_logger Dumpers

Listed below is the contents of the pram.log created by the new hard_logger dumpers on the C3800. This includes the error output from all 19 purge rams. This list includes their names and an error.

As can be seen the error resides in the purge ram ic_valid at location 7b0. The data (1) the data and address validity differ. This should not occur, so the only valid values in these 2 bit registers is a 0, or a 3, indicating the data and address are either valid or invalid. The error occurs when the address and data entries disagree with one another.

The error can be verified by checking the location indicated in the affected ram. A collection of all ram outputs is created in the file pram.stdout. To locate the failure, simply search on the ram name and then the address in the file pram.stdout.

Included with the pram.log is a comment for each ram indicating actual function. These definitions are not included in the actual dump.

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Ram : la_valid	Logical Address Valid
Ram : ic_valid	Instruction Cache Validity
7b0 1	
Ram : br_hist_l	Branch History Cache read data lower word
Ram : br_hist_xl	Branch History Cache read data lower word
Ram : br_hist_u	Branch History Cache read data upper word
Ram : br_hist_xu	Branch History Cache read data upper word
Ram : pte_mod1	PTE Cache odd modified bits
Ram : pte_ref1	PTE Cache odd referenced bits
Ram : pte_tval1	PTE cache odd thread validity
Ram : pte_val1	PTE cache odd validity
Ram : pte_mod0	PTE Cache even modified
Ram : pte_ref0	PTE Cache even referenced
Ram : pte_tval0	PTE Cache even thread validity
Ram : pte_val0	PTE Cache even validity
Ram : dc_tval1	Data Cache odd thread validity
Ram : dc_val1	Data Cache odd validity
Ram : dc_tval0	Data Cache even thread validity
Ram : dc_val0	Data Cache even validity
Ram : sr_val	Scratch Ram validity

Al,

3.10.1 C3400 CPU Soft Errors

There are a category of hardware errors on the C3400 that will be treated as soft errors with the installation of Processor Diagnostics and Database V1.1. These errors (an 1120 External PTE Cache Error is one of these) will be logged in a file on the spu, /mnt/softlog_jcpu.

If a CPU soft error is detected, this event is noted in a memory resident database in addition to the softlog_jcpu log on the spu. If a second error of the same type is encountered in less than 5 minutes, it is then treated as a hard error, and the system will be halted.

This release also requires that V6.0 or later of SPU OS and I/O diagnostics V1.0 be installed.

It is important to install this release of the diags/ddb as soon as possible, since this will ensure that these errors do not interrupt the customers operation.

Dave

3.10.2 Part Number Change for C3400 Multivolt PS.

The part number for the multivolt power supply has been changed. The new part number for the C3400 Multivolt supply is 500-000339-200. If you ordered a spare under part number 500-000339-290, this part can be used, but you will have to remove the tray and mounting hardware from the old supply to install it on the new power supply.

Power supply part number 500-000339-200 is a complete assembly with the tray and mounting hardware installed.

Dave

3.11.1 C2XX PI2 Hard Error Codes

Here are the PI hard error codes that you may not have in your error list.

PI2 Hard Error #651 invalid arbitration queue value
arb_ramchk0 %x arb_ramchk1 %x

PI2 Hard Error #652 PCM RAM parity error
addr<31..22>: %03x data: %0x par: %0x

PI2 Hard Error #653 EBUS read data parity error
rdata_hi %x rdata_lo %x rpar %x\n",
parity error byte(s) - ones are bad bytes - LS to MS

Dave

3.11.2 C3400 CPU Board Interchangeability

Part number 2236 and 3236 CPU boards for the C3400 processor are functionally equivalent and can be interchanged without problems. Part number 1236 CPU board can not be used in place of the 2236 or 3236 CPU boards, however a 2236 or 3236 CPU board can be used in place of a 1236.

Dave

3.11.3 Loading PETS through the SPU on a C3800

The facility for loading PETS through the SPU can be accomplished, but is cumbersome.

If the DAT tape is made in Dallas, then it will arrive compressed. This will save some time, but the DAT tape can be created in the field. I will detail both procedures below.

When the DAT tape has been created for this purpose, then there will only be a single file on the tape. This will generally be labeled pets.tar. This tape should be loaded in the sst partition with the command tar xv. The /sst partition should be used because this is the only one large enough. After loading this file it is then possible to spu -r this file to the OS level and extract the contents of the file by executing "tar xvf pets.tar". This will create the PETS directory exactly as if it had been loaded in a conventional manner.

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If this pre-compressed tape is not available the following procedure can be followed to get PETS to the OS.

1) Copy PETS to the DAT tape by tar
2) Copy DAT contents to /sst by "tar xv
3) create pets file by " tar cvf pets.tar PETS". This will create the file /sst/pets.tar.
4) Boot OS and from the mnt directory execute "spu -r sst/pets.tar".
5) Breakout PETS from the file by "tar xvf pets.tar".

This procedure will accomplish loading PETS so that it can be executed.

Al,

3.11.4 Isolating swip and NCU failures

It can be very difficult distinguishing swip problems from basic NCU failures with out the right knowledge. This task can be made much easier with the following information.

If the diaginit cannot be completed, there are no tools available to help in the diagnosis of a failure in the Swip/NCU loop. In order to clarify some points it is necessary to understand that there are accessible registers on the NCU. Particularly, there are loopback registers that are accessible for the swip. These registers are 210 and 214. The register 210 is actually the loopback register and 214 is the NCU header register.

If there seems to be nothing going on from the spu then it is possible to write and read these registers by the following method.

1) get 0x210
   0x210 ff68c210 maybe returned (This will vary)

2) put 0x210 0x12345678

3) get 0x210 210 0x12345678 (return)

If the proper value is not returned from these registers then it is very possible that the NCU has failed. This will generally happen if the NCU is not powered up. If the value only partially changes then there maybe a swip or swip cable failure.

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It is important to know that the swip registers must be cleaned up before this can be accomplished. This was discussed in tech bulletin v3w5. If this is not accomplished then the results may lead to invalid conclusions.

Al,

3.11.5 Verification of C3800 Clock Cable Connections

In order to insure the proper connection and position of the clock cables it is advised that the utility sysreset -s be utilized. This will initialize the scan engine and if successful will indicate properly installed cables.

The correct installation of these cables will be with connector on the I/O backplane with A up. For the individual bays A will go into location J5 and the B cable will install in location J4 of all bays, including the crossbar.

To establish any kind of scan link it is necessary to have the clock cables installed in the I/O bay and the crossbar at a minimum.

The new x version of spu4000, released with x1.0.0.10 of diagnostics will verify clock cable polarity in subtest 615.

Al,

3.12.1 C3800 Diagnostic Bugs

The following are diagnostic bugs observed with Systems Diagnostics V1.0.

1. cpu4332 - At 16 ns this diagnostic will fail. If you put the osc_freq to 18 ns, this test may be used to help isolate a fault.

2. ncutestall - D4 of this script fails with the following message.

   FAILED ncutestD4
   Fails TRPCMD lock testing.
   Check DLCK CNT2, L2_LCKLCKB, L3_TRPLCKB, L2_TRPLCKB, TRP_BSY, ITC_INT, and CTL_TRP_LCKB.

3. xbinteg e - Fails with the following message.

   TESTING - SENDSEL = 0
   ERROR: xrte:rctl.rm1_rdy = 0x0 (expect 0x1)
   ERROR: xrte:rctl.rm2_rdy = 0x0 (expect 0x1)
   ERROR: xrte:rctl.rm3_rdy = 0x0 (expect 0x1)

4. xbinteg o - Fails with the following message.

   TESTING - SENDSEL = 0
   ERROR: xrto:rctl.rm1_rdy = 0x0 (expect 0x1)
   ERROR: xrto:rctl.rm2_rdy = 0x0 (expect 0x1)
   ERROR: xrto:rctl.rm3_rdy = 0x0 (expect 0x1)

Jerry

3.12.2 C3800 SPU (OPUS) Service Guide

There is now a released version of the C3800 SPU (Opus) Service Guide.

If you maintain a C3800, you will want to order one.

SPU Svc Guide 1.0 C3800 Series - 081-019730-000 Feb 1992 - DHW-304

Dan Brenner

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3.12.3 Verifying C3800 Control Stores

The proper procedure for verifying control stores on a C3800 is to execute "sysreset -l 2 -v". This will load and verify all system control stores on each head.

Al,

3.12.4 C3800 Front Panel Switch Problem

It should be understood that the current front panel switch key is only removable in the off position and not in the secure position. This is an oversight and is being corrected with the release of a new switch. This switch will be cut in on an ecn and will be installed in all currently installed systems.

Al,

3.12.5 C3800 Diagnostic V1.0 Changes

The first production release of c3800 diagnostics is v1.0. Below are a list of changes and enhancements over preliminary releases:

NOTE It should be understood that v1.0 contains new firmware that must be downloaded on installation. This will require a longer installation time dependent on configuration. Please plan accordingly.

1) Diaginit now executes st_311 (Register loopback test) of spu4000. This will verify swip to CU communications. Correctly terminates if XBAR or CU fails to power up. Fixed failures in correct problem reporting.

2) Added scan ring verification of memory boards as each board is powered up.

3) Changed display of the utility dump_soft_log, for memory soft errors. Also corrects known problem of incorrect NMB display.

4) The utility dumptemps created to log system wide temperatures. This is invoked by the hard logger and can be run manually at any time.

5) The utility fw_rev_update is modified to display latest revisions of power system firmware. This is true for the utility ucode_rev_update as well.

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6) Margin command no longer uses osc_freq output to override user selected clock. This now allows clock margining during testing. Also modified margin to verify the CU is up before margining clocks. In the past this could generate a system hang.

7) Allows dumping of all core files and dumpers in the directory /sst/crash to prevent filling the root partition.

8) Initialize the printer port.

9) Added script "set_busses" in /diag/db to provide the ability to alter voltage set points on a permanent basis. In the past the utility altsetpts was good until next boot of system.

10) Sys_shutdown is enhanced to verify that BPC channels are closed. This will ensure total system shutdown. In the past it was possible to complete sys_shutdown with one, or more bays left powered up.

11) Xsfp now monitors and starts required daemons. These include sdb_startup, bpccommd, bpcwatchd and errlogd.

12) Modified xsfp to disable workstation logins when the switch is in secure.

13) ConvexOS will not attempt to boot if already in vmunix.

14) Modified initall and sys_config to display clock values as nominal, upper and lower instead of value. The script osc_update is now installed with the position nominal.

15) Modified mxmrc to support csh xterm.

16) Fixed problems with all cpu diagnostics. All now are executable. Default parameters will be dcache enabled, forced faults off and register display on failures. In addition all cpus will be selected unless modified.

17) The diags cu4000 and mem4000 are enhanced.

NOTE ALL DIAGNOSTICS ARE NOW FUNCTIONAL AT NOMINAL VALUES.

18) Spu4000 is now included in xdiags. This will eliminate the previous spu4000 interface. All subtests now function and subtests 614 and 615 have been added. Subtest 614 is a ring verification of system and log rings for the IA and memory boards. Subtest 810 is now a combined set of system wide continuity tests. This includes subtests 811 and 812.

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19) Modified bpccommd to allow the date to be modified on the SPU. In the past this would cause the complex to power down.

20) Enhances power subsystem tolerance to swis related failures.

21) Modified cdb_browser to correct string display problems.

22) Increases timeout value for cop writes to SWIS and SWIP so that variations for various boards is accounted for.

23) Fixes edit problem in rmtdiag.

24) Modified calculation of system configuration. Now uses os_req fields when determining board availability.

25) Prevents errintd from terminating prematurely during failure. Fixes failures associated with Memory soft errors. Prevents reinitialization of memory after hard errors. This will allow further memory analysis.

26) Corrects failure of utility mmap to display correct physical address.

27) Fixes mminit to allow proper interleave of memory boards of dissimilar size.

28) Fixed infinite loop failing with pwr_util.

29) PPC firmware rev 2.6 corrects intermittent failure to power up crossbar.

Al,

3.12.6 Opus Disk in a RDS Subsystem

When installing the Opus disk in a RDS subsystem, in conjunction with a C3800, it should be understood that the disk will not indicate a ready state and cannot be write protected. The drive is available when the start indicator ceases to flash. The drive will function normally in all other ways.

Al,

3.12.7 Changing the Timezone on Opus Workstation

The easiest way to modify the timezone on the Opus workstation is by executing the utility /usr/etc/install/sys_config. This utility will prompt for pertinent SPU information such as network availability, node name, date/time and time zone the system will exist in. This utility is response driven, so requires no arguments to the command.

Al,

3.12.8 Opus Depends on C3800 Free Running Clocks

It has been discovered that the Opus, or more precisely swip, is dependent on free running clocks on the C3800. If the clocks are interrupted, or the NCU is interrupted for any reason, this can result in a crash of the Opus. Generally this crash will give very few other indications, except for the crash. Some details may be obtained by use of the display_log, or the '/var/adm/messages' file resident on the Opus.

A loose or misfitting swip to ncu cable may also result in clocks being interrupted to the swip and thus create the same type of crash.

This problem can become particularly problematic during the installation phase, as the clocks and clock cables are in a somewhat unknown state. This possibility should be considered when facing successive Opus related crashes.

NOTE It should be understood that Opus crashes do not always result in a crash of the C3800, until the SPU is rebooted. Rebooting the Opus will result in a system wide reset and bring the system down, hard. Because of this, it is advisable to verify that the system is not up, before rebooting the workstation. If the system is still up then it may be possible to schedule the outage with the customer.

It should, also, be remembered that the swip is subject to thermal failure during the Opus boot process. This type of problem can result in a loss of 10 to twenty minutes while waiting for the transceivers to cool down. More information on this failure is available in Tech Bulletin v3w9.

It should be noted that it is necessary to do a general cleanup of the swip registers after a crash, or a failed attempt to diaginit, or boot. This cleanup can often be accomplished by issuing two successive "cleanup' commands at the spu prompt. If this does not clear all registers it will be necessary to manually change the contents. More information on this is located in Technical Bulletin v3w5.

Al,

3.12.9 C3800 Utilities

As with other CONVEX systems, there are other utilities available on the C3800 to assist in further analyzing crashes and hangs. Some of these utilities are described below:

1) xbar_err -
   Assists in further clarifying xbar related failures. This is particularly helpful when the crossbar involvement is not clear. Errors that involve both even and odd return boars can generally be ignored as these usually accompany data dependent failures.

2) nmb_errs -
   Can be helpful in evaluating memory failures. This is very similar to the mcm_func display mcm_errs. This utility can only be executed on a single NMB at a time. The format of the command will be "nmb_errs x" where x is the nmb location 0-7.

3) icach -
   Used for dumping the icahe on an individual head. Very similar to same utility on the C2. Parity errors are portrayed by an *. The format of the command is "DCPU = x ; yyyyyyyy zzzzzzzz" where x indicates the NSP to be dumped 0-7, y indicates the first cache address and z indicates the last address to be dumped.

4) dcach -
   Same as above for display of the dcache. The highest address in the dcache is 3ffc.

5) ptecach -
   Same as above, for pte cache dumps.

6) rcque -
   Used to display returned data from memory. Displays last 24 even and odd words. Very similar to the return queue display on C2. The format of the instruction is "export DCPU = x ; rcque" where x is head to be examined.

7) hang -
   Displays useful info relating to the state of an individual processor. This utility is very similar to same C2 display under iscn. The instruction is in the same format as rcque, above.

These utilities should help in analyzing future system crashes and hangs.

Al,

3.12.10 Multi-head Troubleshooting Utilities

As most everyone knows, there are a couple of utilities available on all CONVEX multi headed systems that can be very useful in troubleshooting.

These utilities are mpa and cpuconf.

They can be especially useful in chasing application failures, wrong answer problems or most any other type of problem where the system does not crash and could be individual head dependent. Both utilities have the convenience of functioning at the OS level and so preventing lost time with reboots to use the spu disable utility. In addition, there are situations where disabling the head at the spu and thus not loading microcode can actually lead to false conclusions.

The utility, mpa, is useful in locking a process on to an individual head. In this way the heads can be isolated with the particular application one at a time and very quickly. You can even have the user, or operator perform this function. The format of this utility is as follows:

mpa -c x application script <where x is the processor from 0-7)
an example would be "mpa -c 1 run < input file"

The utility, cpuconf, performs opposite to mpa. This will allow you to remove a head from scheduling and thus run an application on all heads except one. This can be helpful in isolating parallel application failures. The format of this utility is as follows:

<prompt> cpuconf -d 0
<prompt> run < input file > output file
<prompt> cpuconf -e 0 -d 1

where -d switch is used to disable the head on line and -e is used to enable a head. As can be seen, it is permissible to operate both functions on any number of heads simultaneously.

Use of these utilities can save many hours of unnecessary labor and also prevent unwanted customer down time. These utilities can be run while the customer is using the system.

Al,

3.12.11 FDDI Loopback Tests

It is not possible to run conventional loopback tests on FDDI with the Optical Bypass Switch (OBS) installed. This is because the OBS is installed in such a way as to bypass the conventional wiring configuration. The OBS is used to reroute around a failed system.

In order to run the loopback tests (subtest 2000 and 2010), it is only necessary to exchange the receive cables, on the FDDI controller, between physical A and physical B. In other words move receive B to receive A and vice versa. This will establish a loopback path through the OBS and thus eliminating the need for the loopback connector.

For a more thorough explanation and drawing showing the location of physical A and B, please see the Tech Bulletin v2w44.

Al,

3.12.12 Isolating Wrong Answer Problems

Wrong answer problems can be a particularly nasty problem to locate and correct on a CONVEX system. Although much of this process can be used on any CONVEX system it is specifically written for the C2 (3200) class system. The plan that I recommend here is based on experience in handling many similar problems over the past few years. It is intended to be a general guideline and may need to be altered to cover specific situations.

First, I must stress the virtue of imagination and patience here as these problems are never easy, as the system does not crash and quite often the symptoms appear intermittently, but never randomly. Because the symptoms are not random, this can be used in your favor as most of the effort will entail finding a usable test and proper margin conditions to recreate the proper environment and thus symptoms, as rapidly as possible.

Conventional tools and analysis methods will not be useful in this situation as our current tools are constructed to assist in hangs and crashes.

It should be remembered that many wrong answer problems are temperature and timing related, so, alternately cooling and heating can assist in the process.In addition, margining clocks and the power supplies to increase, or decrease performance will be a great asset.

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Many wrong answer problems become more repeatable after warming up and with margins of high clock +5VDC and -2VDC and low -4.5VDC. In other words uuul. These margins create the fastest throughput and the most noise on memory and I/O. A particular diagnostic selftest may be helpful here. PETS may also be helpful in this situation. Particularly some of the diagnostic messages.

The following isolation process is recommended:

1) Use the mpa and cpuconf utilities to see if the problem is isolated to a particular area of the system.

2) Determine a test and conditions that will fail consistently. This will involve finding the application that fails easiest, on the head that fails quickest and with the most reliable margin conditions.

3) If the problem appears to happen equally on all heads it is possible that an I/O problem may exist. So, running tests simultaneously on different disks and stripe combinations may help in further isolating the failure. IDC's can often cause wrong answer problems by corrupting databases and this may go undetected by the I/O subsystem, but creating a test that runs on multiple file systems and IDC's will quickly isolate this type of failure.

4) You might want to just reload the ddb and diags here. This will only be of help if the system appears timing sensitive. If the system is heat sensitive then this will be of little help.

5) Reduce the system to its lowest common denominator. In other words, physically displace all memory boards after the first pair and remove all but one head. In the case of a wide body this will be head A. This reduction will serve two functions. First, it will reduce the area that has to be examined in the quickest time and second, it will keep other boards from undue stress from powering up and down. This will serve to reduce problems after you have located and fixed the wrong answer problem. Frequently failures can result after an extended test process and removing unnecessary parts will reduce this. It also reduces the real estate on the backplane that must be considered.

6) While looping on your test, use a small piece of credit card, or other non-conductive material to stroke the backplane nets. Using the card in an up and down and side to side motion, being careful to limit the area of coverage. The hope with this is that the problem would be a near pin to barrel open and this will cause a crash. If this happens you're in luck. As a side note, it is recommended that testing for this type of failure be accomplished with a female pin as a meter lead, as this will enable you to gain better control and movement of the pin.

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7) Next, if none of this has helped then you are probably searching for a high resistance net from point to point. This would be defined as any net exceeding .9 ohms on one side of the backplane, or one that exceeds 1.6 ohms that runs along both sides. Keep in mind that flex connectors often fail in this manner. If the system appears to be heat sensitive, a good heat source, or some freeze spray may be may help.

NOTE The most likely source of defective nets that can cause this are memory related data and parity lines. If the problem occurs across all heads then the memory to PI nets should be suspect.

Likely causes of wrong answers follow:

1) high resistance backplane nets (point to point).
2) Low values to vtt, in the 40 to 45 ohm range.
3) VPD's because of termination. It doesn't matter if the application is vector intensive.
4) Microcode
5) IDC, because of undetected data corruption.
6) ASP because of memory interface and control stores.

Al,

3.12.13 PETS Startup Problem

It is possible that after installing PETS that the scripts will appear to start, but no load will be achieved. This is usually because PETS has been loaded under different directory than was intended. The directory used is /mnt, but tapes in installsw format will prompt for the necessary directory during install and thus make path name modifications to the scripts. In cases where PETS is installed in tar format, such as C3800's, it will be necessary to load the tape under /mnt, or modify the run scripts with the different path name.

Al,

3.12.14 PIGA Errors

The error below indicates a parity error in a Pbus read operation, or a bad address as a result of an incorrect pte. As this is occurring during a read, I would suspect a failure prior to the Pbus, such as PIA, Memory, or PTE mechanism. This error could probably be equated to a PI602, but being reported by the CCU.

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The PIGA is the Pbus Interface for all of the differential CCU's. This device replaces the cache that we have on the MIOP, or VIOP.

```
[SPU @00:25:23] <Wed Oct 16 1991>
[CCU03@01:53:28] ERROR: dsk_read_error - PIGA encountered error
[CCU03@01:53:28] PIGA status register 0x00000801
[CCU03@01:53:28] Buffer addr 0x617c0000
[SPU @01:53:28] mm_sniff: 68000 dtack timeout error @ addr 0x41081000
[SPU @01:53:29] mm_sniff: sniffing of pcm block 520 disabled
[SPU @01:53:30] mm_sniff: Fatal error. Sniffing terminated.
[SPU @01:53:35] errintd: **** SOFT ERROR DETECTED ****
description follows...
[SPU @01:53:35] PI2[0]: PBUS transfer error:
[SPU @01:53:35] PBUS arbiter detected reference to non-present memory
[SPU @01:53:36] Error transfer source: CCU[3]
[SPU @01:53:36] hard_logger: WARNING. No Hard/Soft error interrupt pending.
esr=0x500ff
[SPU @01:53:36] hard_logger: Hard/Soft error interrupt source unknown.
[SPU @01:53:36] esr/sel=0x0/0x0
[SPU @01:53:36] CCU2/TLI: Unsupported CCU type
[SPU @01:53:37] hard_logger: Can't isolate Hard/Soft error.
[SPU @01:53:37] errintd: hard_logger exit status: 1
[SPU @01:53:37] errintd: Log of Hard error unsuccessful
[SPU @01:53:37] errintd: Fatal error (status 25). Cleaning up ...
[SPU @08:06:17] Errlog started: -l /mnt/errlog
[SPU @08:06:17] <Wed Oct 16 1991>
```

Al,

3.12.15 C3400 Diagnostic Failures

1. The iscn test script "cuj_scan" may fail due to a missing directory, "logdir." The test "sib_tim_tst" will fail with V1.1 of the diagnostic and spu unix 6.1.

   To run "cuj_scan" with the new diags and spu unix you need to do the following:

   spu> cd /hw/cputest/test
   spu> mkdir logdir

   Ignore the failure in the test "sib_tim_tst."

2. For C3400-ES only. cpu4333 subtest 1005 will fail. Ignore this one subtest failure.

3. cpu4331 C3400-ES only. cpu4331 subtest 43 fails with a cpu in slot 2.

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4. cpu4331 C3400 only. cpu4331 chained mode with multiple cpus will fail when there is no JCPU in slot 0. Causes a firmware reported hard error.

5. Test cpu4041 st 566 will time out running with one head.

6. PETS test.041 will fail. This test is not ran via any of the PETS scripts other than "nmul."

Thanks to Frank Chaney and Mark Jones for this information.

Dave Muir

3.12.16 Error in SCSI V2.1 Installation Instructions

We received an install report recently where an FE voiced concern over the fact that the SCSI V2.1 installation procedures says that a sysgen will be performed, yet 10.0.X OS does not to do a sysgen.

Rather than go through the ECN process to add a DREADED READ ME FIRST, we are notifying the field in the Technical Bulletin of the error in the SCSI V2.1 installation procedure.

The information is incorrect where is states that a sysgen will be done during the installation. With ConvexOs V10.0.x no sysgen will be done.

Thanks, Bee-be & the Install Quality Team

3.12.17 swip/swis Register Bit Definitions

The following is a list of bit definitions for all of the swip/swis registers. These individual outputs can be obtained by doing a get at dshell on the Opus of the individual register.

swip_bsrc_msb:	16#00
swip_bsrc_lsb:	16#10
swip_force_par_err:	16#00
swip_misc:	16#00
swip_int_level_ctl:	16#90
swip_int_ena:	16#80
swip_int_stat:	16#00
swip_force_int:	16#00

.....continued on next page.....

```
swip_bsrc_msb
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    # Inv| Int|Re- |NCU #    PERR
|                  unused            #Addr|Lock|run |Err #

swip_bsrc_lsb
VALUE: 16#10
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    # Inv| Inv| INV|Err
|                  unused            #Addr|Size|Req |Ena


swip_force_par_err
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #ILck|SOFT|    |    #
|                  unused            #Test| LOG|ADDR|DATA#    FORCE

swip_misc
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    # NXP|ADDR| NCU|RRun#
|                  unused            # ENA|ONLY| RES|Ena #

swip_int_level_ctl
VALUE: 16#90
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |    #UART|UART|UART|UAR
|                  unused            # NCU| EXT|MODM| SPU#  3 |  2 |  1 | 0

swip_int_ena
VALUE: 16#80
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |          Reserved
|                  unused            # NCU| EXT|

swip_int_stat
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |          Reserved
|                  unused            # NCU| EXT|
```

.....continued on next page.....

```
swip_force_int
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |          Reserved
|                 unused             # NCU| EXT|

swis_bsrc_msb:        16#00
swis_force_par_err:   16#00
swis_misc:            16#0a
swis_int_level_ctl:   16#90
swis_int_ena:         16#1f
swis_int_stat:        16#00
swis_force_int:       16#00
key_switch:           16#17

swis_bsrc_msb
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    # Inv| Inv| Inv|
|                 unused             #Addr|Size|Req |

swis_force_par_err
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |SOFT|
|                 unused             # RES| LOG|       RES

swis_misc
VALUE: 16#0a
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #          |Uart|    #
|                 unused             # RES| RES|Rst |BPC4#BPC3|BPC2|BPC1|BPC0

swis_int_level_ctl
VALUE: 16#90
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #Mstr|       Interrupt Level
|                 unused             # Ena| 07 | 06 | 05 # 04 | 03 | 02 |01

swis_int_ena
VALUE: 16#1f
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |    #UART|UART|UART|UAR
|                 unused             #      RES     | Key#  3 |  2 |  1 | 0
```

.....continued on next page.....

```
swip_int_stat
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |    #UART|UART|UART|UAR
|                unused              #      RES     | Key#  3 |  2 |  1 | 0

swis_force_int
VALUE: 16#00
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
|                                    #    |    |    |    #UART|UART|UART|UAR
|                unused              #      RES     | Key#  3 |  2 |  1 | 0

key_switch
VALUE: 16#17
| 15 | 14 | 13 | 12 # 11 | 10 |  9 | 8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 | 0
                                     #   MODEM    #       SPU
```

Al,

3.13.1 C3800 Modem Replacement Procedure

To replace the C3800 modem without bring the SPU down, first power down the old modem, replace the old modem with the new modem, then:

1. Log into the SPU as root
2. Using an editor, edit the file

   /etc/ttytab

   setting ttya to off.
3. Write file /etc/ttytab.
4. Enter:
   spu> kill -HUP 1
   spu> /diag/bin/modem_init
5. Using an editor, edit the file

   /etc/ttytab

   setting ttya to on.
6. Enter:
   spu> kill -HUP 1

Jerry

3.13.2 C3200 Diagnostic Bug

On the V5.0 C3200 Diagnostic and Database tape there is a bug with cpu4233 subtest 401. The test will fail on C3240's with MCM's. It will pass with MCM3's or on cpu configurations of less than 4 heads. The test fails with an unexpected exit instruction (a1 = 0x5008 a5 = 0x0) from the control cpu.

There will be a fix to this test on the V5.1 tape which is due to be ECN'd the third week of April. Thanks to Mark Jones for this information.

Dave Muir

3.14.1 Subject: C3800 spu4000 connectivity test

(signals not covered in current release)

This does not include any scan or clock related signals in the list.

Memory Board <-> Xbar	Tested Where:
mb_xc.soft_error	spu4000 st_710-713
mb_xc.hard_error	spu4000 st_710-713
mb_xc.ram_rfsh	mem4000
spares n/a	

Scalar Processor <-> Xbar	
xc_sp.trap_type<0-3>	
xc_sp.trap_vec<0-11>	
xc_sp.usec_en	
xc_sp.deadlock	
xc_sp.cu_status_en	
xc_sp.cu_status	
xc_sp.mt_comp	
xc_sp.trap_rdy	
sp_xc.stop_cntr	spu4000 st_710-713

Vector Processor <-> Xbar	
vp_xc.hard_error	spu4000 st_710-713

NCU <-> Xbar	
xc_cu.trap_type<0-3>	
xc_cu.trap_vec<0-11>	
xc_cu.trap_rdy<0-8>	
xc_cu.status_psel<0-3>	
xc_cu.status_en	
xc_cu.status	
xc_cu.deadlock<0-7>	
xc_cu.trap_comp<0-8>	

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xc_cu.usec_en
cu_xc.usec_en
cu_xc.xcl_addr<0,2,3,4>
cu_xc.xcl_addr_par
cu_xc.xcl_mux_ctl<0-2>

NIA <-> Xbar

ia_cu.trap_vec<0-11>	
ia_xc.hard_error	spu4000 st_710-713
ia_xc.soft_error	spu4000 st_710-713
xc_ia.status_en	
xc_ia.status	

Thanks to Steve Nevalsky for this input.

Jerry

3.14.2 C3800 Net Resistance Value

It should be noted that any data net on the C3800 that exceeds 56 ohms should be considered a possible source of failure. Because of the system edge rates, any net that is not double terminated that is above this value can cause intermittent failures.

Causes of nets exceeding this value are normally epont, or augat related. These nets can cause very intermittent failures and can be difficult to locate.

When measuring point to point from heads to crossbar, these nets should measure less than 2.5 ohms. Any net exceeding this value should be viewed suspiciously.

Epont cables should measure less than 1 ohm point to point, with the same cautions as above.

Al,

3.14.3 C3800 diaginit abort

If for any reason that the diaginit process on the C3800 should abort prior to initializing the CCU's, they will not be recognized on the next pass of diaginit. This means that the system will not boot because the CCU's are offline.

.....continued on next page.....

This happens because the CCU's share power with the NIA and this has been initialized on the previous pass. In order to get the CCU's initialized on the second pass of diaginit, it is only necessary to powerdown the NIA and then execute diaginit. This will pickup the missing CCU's.

With the installation of v1.0 of the diagnostics, it is a very common situation for the diaginit process to abort after the spu4000 subtests are executed. This is not a cause for alarm and only requires diaginit to be rerun. But in these situations the above information will keep you from having to accomplish a sys_shutdown.

Al,

3.14.4 Continuity Test Failure Before sysreset

It is not possible to successfully complete any continuity tests, such as sys_con, or xc_con, before a sysreset has been accomplished. All failures from continuity tests should be ignored until after a sysreset has been accomplished.

It is also not possible to complete diagnostics until an initall has been accomplished. In most cases, until the initall is complete the diagnostics will abort with a bus error. But, in some cases the diagnostic will fail after running for an extended period. This is especially true for mem4000.

Al,

3.14.5 C3800 Gate Array Identification

In cases where there are multiple gate arrays, or rams for even and odd data, the gate arrays are distinguished by a 0 and 1. For example the NPA0 and NPA1. The convention is that the 0 indication is for even and the 1 is for odd.

The lone exception to this rule is the NDAT, located on the NCU. This designation is reversed for this device. So, it should be realized that NDAT1 handles even data.

Al,

3.14.6 New IPI Disk Trays

Beginning this quarter, CONVEX has begun to use a new vendor for the IPI disk trays. As a result of doing this there have been some necessary changes.

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The contents of the tray hardware have changed somewhat. Now, included with the trays will be 4 screws (p/n 310-002401-001). Two (2) of these screws will be used to mount the rails together, with the other two screws used to secure the drives to the tray. In addition, 4 gold colored nut bars will be included. It should be understood that the thin side of the nut bar should be mounted toward the center of the cabinet. If this is not accomplished then the tray will not fit properly into the rails.

If there are questions, or recommendations about this new hardware, please refer them to Charles Putman at x4043, or email putman.

Al,

3.14.7 NCU Powered off and mminit Failures

It should be noted that if the NCU is powered off and/or removed from the system individually, there is a possibility of encountering mminit failures after the diaginit.

The mminit failures will be due to a failure with access of the memory test logic (MTL) located on the NCU. This failure can be overcome by executing a sys_shutdown and re-executing diaginit.

Al,

3.14.8 IA Soft Errors and rslog Utility

The following is a display for the utility rslog. This utility can be very helpful in locating the source of IA soft errors and mminit failures, found on C3800's.

This utility can be executed by entering "rslog" at the SPU prompt.

```
                              IA8 soft log ring
    |     parity errors (bytes)       |ill|wrt|rd |wrt|hdr|ccu0|ccu1|ccu |
port| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |hdr|pcm|pcm|pe |pe |err |err |num |
----------------------------------------------------------------------------
nxi | 1   1   1   1   1   1   1   1   0   0   0   0   0   0   0   0
pbi0| 1   1   1   1   1   1   1   1   0   0   0   0   0   0   0   1
pbi1| 1   1   1   1   1   1   1   1   0   0   0   0   0   0   0   1
pbi2| 1   1   1   1   1   1   1   1   0   0   0   0   0   0   0   1
pbi3| 1   1   1   1   1   1   1   1   0   0   0   0   0   0   0   1
```

Al,

3.14.9 Running pets on a C3400

Do not run pets on a javelin with other than nominal margins. Running at other than nominal will cause intermittent failures.

This problem is due to a voltage margin problem with the TI gate arrays. A re-design is underway to correct the problem.

Any failures in pets running normal margins should be treated as hardware failures.

Dave Muir

3.14.10 DMM Identification

The part number on some DMM modules may not accurately reflect the amount of memory on the dmm. In order to verify what size the dmm is, check the part number of the memory components.

Motorola parts have part number MCM514400XXXXX - this is a 4mbit part (1m x 4). DMM's with this part will yield a 8mbyte dmm.

Mitsubishi parts are numbered M5M44256XXXXX - this is a 1mbit part (256 x 4). DMM's with this part will yield a 2mbyte dmm.

The important part of the part number is the '256' or the'400'. In the case of both manufactures the 256 and the 400 indicate the size of the ram chips. The 'XXXXX' are date codes, and can be disregarded.

Dave Muir

3.14.11 C3400-ES B3 Errors

Some C3400-ES systems are intermittently faulting with a B3 error code. This is a VME airflow fault in the internal VME chassis. A temporary solution for machines exhibiting this fault is removing the VME chassis cover.

Engineering has determined the cause of the failure, and is working on a solution. A permanent fix should be available in the near future.

Dave Muir

3.15.1 C3400 #1122 Hard Error

If you see this hard error on any of your C3400 systems, please contact the TAC for further information.

```
CPU6/JCPU: [#1122] firmware hard error
CPU6/JCPU:     field              se[0]         se[1]
CPU6/JCPU:     se[].q2_frc_err: 0x00000001    0x00000001   ( 1 bits)
CPU6/JCPU:     se[].tl[0]:      0x0000000b    0x0000000b   (32 bits)
CPU6/JCPU:     se[0].tl[0] indicates a deadlock during idle loop
CPU6/JCPU:     se[1].tl[0] indicates a deadlock during idle loop
```

There is a microcode update that will correct the problem, but the microcode has not finished qualification. The new microcode is available on an emergency basis for sites having this problem.

* Dave Muir *

3.15.2 C34xx Processor Diagnostics and Database Versions

On your next site visit to a customer with any C34xx series system, check the version of the processor diagnostics and database. The most current version is V1.1. A Co-requisite is Convex C200/C3200/C3400 Series I/O Diagnostics V1.0.

This version corrects some diagnostic bugs and microcode bugs, and improves error handling on some C3400 hard errors.

If systems you support do not have these versions installed, I would recommend that you install them as soon as possible.

* Dave Muir *

3.15.3 SPU Unix Version 6.0 Bug

There is a bug in the dump/restore utilities of SPU unix V6.0. The restore utility will not correctly restore a good dump tape. The new version of the restore utility is on SPU Unix V6.1.

* Dave Muir *

3.15.4 Diagnostic database and New mcm3 410-003230-200

This new version of the mcm3 is not included in /mnt/usr/lib/DB_cop prior to V1.1 of C3400 cpu-diags/database. If you do not have the correct DB_cop, the system will not recognize the new mcm3 memory board and will not initialize correctly. As a temporary measure, until V1.1 is installed, you can edit the DB_cop file and add an entry for the new board.

* Dave Muir *

3.16.1 C3800 Spu Console Window Messages

It should be understood that all messages occurring in the SPU Console window on the C3800 workstation do not indicate failures. Many of the, reported, messages are actually status messages and do not, necessarily, indicate a fault that needs user attention. Examples of status messages are as follow:

1) Scalar Halt message while executing subtest 713 of spu4000.

2) Swip Bus Error after execution of cleanup and osclean from the SPU.

3) Intermittent "Framing Error" that indicate a missed transfer from the SWIS and a BPC. This transfer will then retry and correct the situation.

4) Overruns caused by a loss of transfer from the front panel key. Again the transfer is picked up successfully on the retry.

These "status" conditions were ignored in prior releases of the diagnostics and only after installing v1.0 have the conditions been reported. Because of the nature of these messages, it should always be assumed that there is no failure if everything seems to function properly.

Al,

3.16.2 OPUS Failure During Download of SWIP/SWIS

A new problem has become apparent with the Opus. This problem is that the down load of the SWIP/SWIS during boot can fail with a trap. This problem has only recently surfaced and is possibly related to the new 4MB simms installed in the Opus.

This problem will cause the reboot of the Opus to abort with a trap and can only be cleared by powering the workstation off. If the workstation is not powered off the condition will remain, even with successive reboots.

Al,

3.16.3 OPUS Status Utility "sfp"

There is a utility existing on the Opus that is used to find the status of the system and Opus. This utility is called "sfp" and stands for soft front panel.

With this utility it is possible to obtain the key switch position, the SPU printer status and the boot mode of the C3800. The display function is utilized by entering "sfp" at the spu prompt. This will generate the following return:

switch position: LOCAL (or, remote, secure)
boot mode: diagnostic
printer: 0

The printer status is displayed as a 0, as above, or a 1. The 0 indicates off and the 1 indicates the printer is online. To change the status of the printer, remotely, it is necessary to enter sfp -p x, where x is a 1, or 0 depending on the desired state of the printer.

Al,

3.16.4 C3800 SST V2.2.1

The release v2.2.1 of SST has fallen behind system rev levels and will only pack the patterns for the NIA on newer systems. In addition, the NIA will fail hard.

The release v2.2.2 should be released in the near future which will address the current problems. In the meantime v2.2.1 should not be run as there is no chance of success.

Al,

3.16.5 C3800 Diagnostic Failures

Several diagnostic failures have surfaced recently with the C3800 and are reported as follows:

1) IDC4000 will fail subtest 1410, Pbus Access Test.

2) Cpu4333 will not work.

3) Xdiag version of cpu4332 will only execute successfully following an initall, directly preceding the diagnostic execution.

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4) The TOC test with the diagnostic NCUtestall and the xdiag cu4000 will intermittently fail with a stuck status of 2. This can generally be cleared with a sysreset -l2. The failure can be verified by executing usec_check under /diag/hw/cutest on the SPU.

5) Diag cpu4331 will not execute in parallel mode.

Al,

3.16.6 C3800 Diagnostic Enhancements

With the release of version 1.1 of the C3800 diagnostics there are some enhancements and fixes that all FE's should know about. The differences to v1.0 of the diags are detailed as follow. Most important changes will be denoted with *:

* 1) Code added to determine the actual frequency of the system clocks and display this "true" frequency value in the xsys_config display. This replaces the current "nominal, high and low" seen in the display under v1.0. This code will execute at diaginit.

2) Code added to diaginit that will prevent downloading firmware to a board that currently has 300V applied.

3) Changes to diaginit to prevent loading firmware to bpc channel that has been previously opened.

4) Changes made to hard_logger to support CXTS, a -i switch added to ignore rule reduction and a -q added to prevent the hard_logger output from being saved to a file.

5) Installsw will now report progress during the installation process.

* 6) Change to mminit that allows the selection of Memory board sizes and displays in xsys_config. A memory board can only be reduced in size and cannot be made larger than physically possible. The necessary modifications to xsys_config are also included to support this function.

7) Added SWIP/SWIS cop at initialization which will allow these boards to be modified with the 3800 powered off.

8) Additional tests added to subtest 810 of spu4000.

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* 9) Added a CU ring clear routine to st_410 of spu4000. This change will prevent bus errors during execution during diaginit and thus prevent the intermittent failures of diaginit at this point.

10) Added st_615 to spu4000 which verifies system clocks to all boards.

11) code with bpccomd modified to correct message problems due to the bpc-swis cable being incorrect.

* 12) Added check to base I/O cabinet during diaginit that would allow CCU's to be powered up on second pass of diaginit. This will prevent the NIA from having to be powered off after a diaginit failure in order to get CCU's properly scanned.

13) Errintd modified to correctly analyze and clear IA soft errors.

14) Sysreset will reflect the current burst count of XS0.

15) Modification of sys_shutdown to insure that all bpc's power off.

* 16) New ucode, version 4.146, is downloaded with this release.

* 17) New ppc firmware, rev 2.7, is downloaded with this release. Because of this, extra time to load diagnostics should be allowed.

18) Changes to scan rings, particularly XCL, have been accomplished.

19) Diag cpu4331 will now function properly in forced faults.

20) Will download ucode to SP/VP during mem4000 if not previously accomplished. This will prevent failures in class 4 and 5 of this diagnostic.

21) BPC firmware 3.15

22) HiPPI support

Al,

3.16.7 C3800 Microcode Fixes in V1.1 System Diagnostics

The following are two us_ucode fixes contained in the System Diagnostics V1.1 release.

rev4.135 - fixed Icache purges such that they really did 2 clock purges - this would be important on old versions of the PRAM part

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rev4.146 - fixed OS panics while running CSD bug. There was a problem in how the trace traps used in parallel thread debugging was handled.

Jerry

3.16.8 Ultranet Controller Revision Levels

The present usable Convex Revision Levels of the 211-000108-200 and the corresponding UltraNetwork Part Numbers and Revision levels are:

Convex Part Number	Current Convex Revision Level	UltraNetwork Part Number	Earliest Usable Ultra Revision	Latest Usable Ultra Revision
211-000108-200	D	95-0032-001	S	T
		-OR-		
		95-0032-004	T	U

* Dave Muir *

3.16.9 C34XX Microcode Revision Level

The microcode revision on C34XX systems can be determined with the SPU command "cs -r". This will not affect the operation of the system if it is running since it does not read the microcode from the CPU boards.

There is a microcode revision file (UCODE_REV) on the spu that was used with V1.0 and V1.0.1 could be looked at to determine the revision level of the installed microcode. With V1.0.2 and V1.1, this file is no longer used and is not on the release tape.

You can remove the file /mnt/usr/ucode.xxxx/UCODE_REV, where xxxx is 1236 or 2236.

* Dave Muir *

3.16.10 C3400 Cold Startup Problem

A few C3400 systems have exhibited a problem during boot if the system is cold. Occasional failures of clock tune values and microstore verification values have been seen when booting a cold system. This failure happens because the cpu reset fails to correctly reset the processor boards. Engineering is currently working on a solution to this problem.

If you have a system exhibits this problem, allow the system to warm up for about 5 minutes before attempting to boot.

* Dave Muir *

3.17.1 SWIS Error Processing

There are two types of error detecting internal to the SWIS; hardware and software. Hardware errors are errors that require logging in the (1) BSRC.

Software errors are detected through polling status registers internal to the OCTART.

Hardware errors are limited to problems in the SBus transaction. These include:

* Invalid Address - The SWIS was given an address during an SBus transfer that was not mapped to any device or function.

* Invalid Transfer Size - The SWIS received an SBus extended transfer request.

* Invalid Transfer Request - The SWIS received an SBus burst transfer request.

Hardware errors result in the process making the access receiving a bus error signal (SIGBUS). If the process doesn't have a bus error handler, it will be terminated by the kernal.

Software errors are determined through register polling of the OCTART. These include:

* Framing Error - A stop bit was not detected when the data character in the OCTART FIFO was received.

* Parity Error - A parity error was detected when the data character in the OCTART FIFO was received.

* Overrun Error - A new character was received while the OCTART FIFO was full and a character was in the receive shift register.

Software errors are reported by the kernel in the console window. These errors are considered non-fatal, so the kernel attempts to sync back up to the BPC and continue operation.

(1) BSRC (Bus Error Source Register) - Refer to the Chapter IV (SWIP/SWIS) of the C3 Maintenance Handbook for register bit definitions.

Jerry

3.17.2 SWIP Error Processing

There are two sources of errors from the SWIP: internal and NCU. Both of these sources perform error logging in the BSRL and BSRU registers.

Internal errors are limited to problems in the SBus transaction. These include:

* Invalid Address - The SWIP was given an address during an Sbus transfer that was not mapped to any device or function.

* Invalid Size - The SWIP received an SBus extended transfer request.

* Invalid Request - The SWIP received an SBus transfer request.

  These errors result in the process making the access receiving a bus error signal (SIGBUS). If the process doesn't have a bus error handler, it will be terminated by the kernel.

  The NCU may generate several errors. These errors may be encountered when a transaction process is attempted or due to static error conditions related to the state of the NCU.

  Anytime a NCU error condition results in a error acknowledgment being performed (SIGBUS), the SOFT_LOG bit will be set in the PEFR register. Soft Log performs two vital functions: 1) preventing the error processing code in the SPARC SPU from receiving another SIGBUS from some follow on SWIP access before it is ready to handle it and 2) disabling all accesses to the NCU, thus preserving transaction particulars that might prove useful in debugging the problem. The SWIP NCU interface state machine will not attempt a transaction while SOFT_LOG alone is set. The state machine may be re-enabled either by clearing SOFT_LOG, or by also setting CHECK_ERRor. When both CHECK_ERRor and SOFT_LOG are set the state machine will operate, but error acknowledgments will not occur. Each transaction performed under these conditions must be followed by polling of all error reporting bits in the BSRU and BSRL. Once all of the error recovery/correction processing has been performed, the software driver should clear SOFT_LOG, if it is appropriate to do so. This means all error codes have been accounted for and cleared.

* Interlock - The SPU-NCU cable is not completing the interlock connections between the SPARC SPU and the C38XX. The interlock error will not cause an error acknowledgment unless the ERRor-ENAble bit is set in the BSRL. The error will then be reported on the next access attempt to the NCU.

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* Rerun - The RERUN error bit is set in the BSRU any time the SWIP board must time out an access attempt to the NCU. A rerun error should always be followed by a toggling of the RERUN_ENAble bit.

* NCU ERROR - The NCU may issue an error to the SWIP under three different circumstances. Error assertion is the default state of the NCU ERROR signal whenever the NCU does not have power applied to the board; assertion registers on the SWIP provide this default state. The NCU_ERRor bit may only be cleared after the NCU power has been applied.

  The NCU will also assert the NCU ERROR signal whenever it detects a parity or invalid address error in the address header that the SWIP has latched into the NCU. The problem is generally related to hardware transceiver failure on either the SWIP or NCU, or a cable connection problem. A write/read pattern test of the 2x214 Address Loopback Register will usually detect the failed signal.

  NCU ERROR assertion is performed anytime data parity failure is detected on data sent to the NCU by the SWIP during a write transaction. A read of the NCU ERROR LOG register 0x401C will indicate if the data parity bit is set, along with associated parity syndrome bits for the corrupted bytes of the transaction. This error is normally related to failed hardware.

  Operations internal to the NCU and NXP interface on the NCU may cause error conditions to be set in the NCU ERROR LOG. These registered error conditions are logically OR'd and the result sent to the SWIP via the NCU ERROR signal. The NCU ERROR will be asserted during a transaction if one of these conditions has been set. A transaction does have to be in progress for a condition to be set, but the SWIP will not asynchronously act on the assertion. A transaction to the NCU must be in progress before an error acknowledgment will be issued at the end of the transaction.

* PERR - The Parity ERRor bits are the failed parity syndrome check bits for the 4 data bytes during a read from an NCU transaction. This problem is generally related to a hardware transceiver failure on either the SWIP, NCU, or a cable connection problem. A write/read pattern test of the 0x214 Address Loopback Register, will usually detect the failed signal. The PERR bits should never be found set at the same time as the NCU ERRor reporting bit in the BSRU. This condition is usually indicative of a NCU powerdown during a read transaction.

Note: For register bit definitions, see Chapter IV (SWIP/SWIS) in the C3 Maintenance Manual.

Jerry

3.17.3 Opus Workstation Thermal Failures

As previously mentioned in tech bulletin v3w9, the Opus workstation is subject to thermal failures after a boot that usually manifest themselves as a failure to diaginit. As there have been some recent diaginit failures with v1.0 of the diagnostics and there may be more in the future, it may be necessary to verify whether the failure is thermal related, or one of the other possibilities.

The verification is quite simple and involves writing to and reading register 0x214 located on the SPU. This can be accomplished by the following sequence after the diaginit fails:

```
spu> get 0x214
spu> put 0x214 ffffffff
spu> get 0x214
       ffffffff
```

If you are able to faithfully retrieve a pattern deposited in this register then the failure is not of the thermal nature. The thermal problem will inhibit any communications with the NCU. It should also be pointed out that the NCU loopback register, 0x210, no longer functions normally during deposits and fetches. Since v1.0 of the diagnostics it now takes as many as 4 deposits to successfully deposit into this register and frequently entering f's generate 0's in the register. The cause of this failure is unknown at this time and is quite perplexing as this register is used extensively in subtest 310 of spu4000, which is run at diaginit.

Al,

3.17.4 C3800 Auto Reboot Scripts

It should, by now, be very obvious that the auto reboot scripts are ineffective, at best. This is due, primarily, to cleanup problems after the various crashes. Every crash seems to corrupt different system resources and registers, so that finding the "magic bullet" solution to all of these cases is quite difficult.

Additionally, v1.0 of the diagnostics has presented some additional cleanup problems that are hoped solved with v1.1. These problems resulted in failures with diaginit and the cleanup script. It is hoped that v1.1 of the diagnostics addresses the majority of these problems and thus allow a more reliable reboot.

Meanwhile, the auto reboot script has been passed off the diagnostics folks to try and obtain the proper cleanup routines necessary to make it more reliable.

.....continued on next page.....

It is also requested that systems experiencing repeated problems, particularly, the resource underflow and nvrf failures, disable the autoreboot script, as it is imperative that we obtain information on these faults in order to solve them. Even if the reboot script does not get the system rebooted, it will still reset the system and thus destroy data points.

Al,

3.17.5 C3800 Crossbar Power Pallet Nutplates

It should be understood that the nutplates (p/n 320-002189-500) should not be included when returning C3800 crossbar power pallets. The reason for this is that the nutplates have been removed from the bom of the power pallet (p/n 500-0005000-200).

If the nutplate is returned then there will not be one available for the replacement. This would generally not be a problem as the current power pallet would generally not be returned until receiving the replacement, but could be a problem if the bad part is returned first.

Al,

3.17.6 xdiag Interface

Because of the nature of the xdiag interface, it not currently possible to run diagnostics by that method remotely. In addition, because of the unknown state of the diags it is desirable to confirm many of the failures by some other means. Both of these situations can be rectified by the use of ddb to execute diagnostics. This tech tip is intended to provide some basic information and examples for using ddb.

In addition it is desirable to run diags under ddb when further analysis of the failure is desired. This cannot be accomplished under xdiag as there is currently, no way to prevent a cleanup of registers after a failure.

The utility ddb is a debugger and is based on the more familiar debugger, adb. So, anyone familiar with adb will have no trouble executing ddb.

First off ddb is entered by entering ddb at the spu prompt. The return will be as follows:

```
[DDB]->
cpu:0,cir: 0,tid: 0
```

.....continued on next page....

Most ddb commands will be executed by preceding the command with a $. Diagnostic specific commands require no $.

A status can be obtained by the following:

[DDB]->$status

```
+---------+----------+----------+
| Memory  |   Stop   |   Bkpt   |
|  Mode   |   Mode   |   Mode   |
+---------+----------+----------+
| LOGICAL |  NORMAL  |   DIAG   |
+---------+----------+----------+
```

```
+---------+----------+----------+
|  CPUID  | CPUSTATE | BKPTMODE |
+---------+----------+----------+
|  CPU0   |  UNINST  |  PARKED  |
|  CPU1   |  UNINST  | PARKED   |
|  CPU2   |  UNINST  | PARKED   |
|  CPU3   |  UNINST  | PARKED   |
|  CPU4   |  UNINST  | PARKED   |
|  CPU5   |  UNINST  | PARKED   |
|  CPU6   |  UNINST  | PARKED   |
|  CPU7   |  UNINST  | PARKED   |
+---------+----------+----------+
```

Test name = 'NO TEST SPECIFIED' is loaded into segment '0'

data_ffaults = 'OFF'	ip_ffaults = 'OFF'
enable_dcache = 'ON'	vl_count = '16'
seq_mode = 'OFF'	chain_mode = 'OFF'
parallel_mode = 'OFF'	multi_cirs = 'ON'
scn_ovr = 'ON'	secure_mode = 'OFF'

This status will give you the default state of the diagnostics and system if entered before setting any parameters, or will give the current environment that the diagnostics will execute in.

The parameters that can be changed are printed at the bottom of the display and will change when preceded with a test name. These parameters will not need to be preceded with a $.

Some helpful commands follow:

.....continued on next page.....

1) $park - This is used to place a cpu in such a mode as to not interfere with other cpu's in run mode.

2) $idle - This places the selected cpu in a ucode idle loop at the execution of a run command.

3) $q - Will exit debugger.

4) &a? - Display contents of address register. The s and t registers can be displayed in the same format.

5) $halt - Stop clocks when executed with no arguments. Arguments can be included to stop clocks on an individual processor. For example $halt cpu 2.

6) $mmode - Change mode of memory addressing. For example $mmode phys.

7) $status - Generates display, above.

8) $r - Display contents of general registers of current cpu.

9) $R - Display contents of general registers for all cpu's in complex.

10) $> - Redirect output to named file.

The following are example of executing diagnostics under ddb:

********** sequence to start forced faults 4041 on heads 0 and 1 ******

```
$clear
$test cpu4041 0  ## The 0 indicates the segment of memory to load the test
$run 0 1
$dcpu 0
$dcir 0
vl_count/=w 10
Forced_faults/=w 1
Chain_mode/=w 1
$dcpu 1
$dcir 1 vl_count/=w 10
Forced_faults/=w 1
```

.....continued on next page....

```
  Chain_mode/=w 1
  Chain_entrypoint:r

********** sequence to read heads 0 and 1 current subtest *************
  $dcpu 0
  $dcir 0
  Current_subtest/w
  $dcpu 1
  $dcir 1 Current_subtest/w

****************** regular 4041 heads 0 and 1 ***************************
  $clear
  $test cpu4041 0
  $run 0 1
  $dcir 0
  $dcpu 0
  vl_count/=w 7f'
  Chain_mode/=w 1
  $dcir 1
  $dcpu 1
  vl_count/=w 7f
  Chain_mode/=w 1
  Chain_entrypoint:r

  ************************Head 3 ************************

  $clear
  $test cpu4041 0
  $run 3
  $dcir 3
  $dcpu 3
  $park 0
  $park 1
  $idle 2
  vl_count/=w 7f
  Chain_mode/=w 1
  Chain_entrypoint:r
```

Al,

3.17.7 C3400 Cold Startup Problem Clarification

A few C3400 systems have exhibited a problem during boot if the system is cold. Occasional failures of clock tune values and microstore verification values have been seen when booting a cold system. This failure happens because the cpu reset fails to correctly reset the processor boards. Engineering is currently working on a solution to this problem.

| If you have a system exhibits this problem after being powered down, allow
| the system to warm up for about 5 minutes before attempting to re-boot.
| After allowing the system to warm up, re-start the system with /etc/reboot
| and start the boot from the fp> prompt. Do now power the system back
| down.

Thanks to Dave Horak for the additional information

* Dave Muir *

3.18.1 Running spu4000, cu4000 and mem4000 Remotely

As ddb cannot be utilized to activate spu tests (spu4000, cu4000 and mem4000, you must utilize dsh if you want to run these tests from a remote location.

The following are some examples of dsh test methods. This is not intended to cover all situations but should provide enough to cover most. All entries after the xxx> prompts are entered by you.

---

1. An example of running cu4000.

```
spu> cu4000

+++>
<Thu Mar 26 12:41:45 1992> cu4000:../../cti.c:242
Test Start (DiagER299): Test Startup Event

test name: cu4000
cwd: /users/diaguser
cmdline: cu4000
****
STARTUP> sub_all *(This will ensure that all subtests are run)*
subtest class description                                    timeout dep
  100       1 Communication Register Parity Error Generation.   45
  105       2 Communication Register Lock Bit Test.           1000
  110       2 Communication Register Pattern Test.            1000
  115       2 CU Control Space Test.                            45
  120       3 Communication Register Functionality Test.       300
  200       3 CU ASAP Logic Testing.                            45
  210       3 CU RDCMR/WRCMR Testing.                           45
  220       3 CU TOC and ITC Functionality Testing.             45
  230       3 CU Deadlock and Firmware Traps Testing.           45
  300       3 CU Interrupt Test.                               120
STARTUP> run *(Starts the test)*
info: "cu4000 subtest 100 running"

+++>
<Thu Mar 26 12:42:25 1992> cu4000:../ncu4000.c:137
SW Info (DiagIN230): Test complete
```

.....continued on next page.....

```
Test: cu4000 R1.0 Subtest: 100 R1.0 Class: 1
Purpose: Communication Register Parity Error Generation.
***** SUBTEST SUCCESSFULLY COMPLETED *****
****
info: "cu4000 subtest 105 running"
***** Now testing lock bit 0000 *****
***** Now testing lock bit 0100 *****
***** Now testing lock bit 0200 *****
***** Now testing lock bit 0300 *****
***** Now testing lock bit 0400 *****
^CPRE-CLEANUP> exit *(At this point the test was stopped with a ^C
                     then did an exit)*

+++>
<Thu Mar 26 12:44:05 1992> cu4000:../../CTIsequencer.c:469
Test End (DiagER316): CTI Test Summary

test name: cu4000
runtime: 1:26.246
subtests started: 2
subtests passed: 1
subtests failed: 0
****

+++>
<Thu Mar 26 12:44:05 1992> cu4000:../../CTIutil.c:229
Test End (DiagER300): Test Termination Event

test name: cu4000
status: PASSED
****
```

---

2. An example of running selected subtests of mem4000.

```
spu> mem4000

+++>
<Thu Mar 26 12:50:19 1992> mem4000:../../cti.c:242
Test Start (DiagER299): Test Startup Event
```

.....continued on next page.....

```
test name: mem4000
cwd: /users/diaguser
cmdline: mem4000
****
ERROR "CPU 0 is not available for testing"
ERROR "CPU 1 is not available for testing"
ERROR "CPU 2 is not available for testing"
ERROR "CPU 3 is not available for testing"
ERROR "CPU 4 is not available for testing"
ERROR "CPU 5 is not available for testing"
ERROR "MB 0 is not available for testing"
ERROR "MB 1 is not available for testing"
ERROR "MB 2 is not available for testing"
ERROR "MB 3 is not available for testing"
ERROR "MB 4 is not available for testing"
ERROR "MB 5 is not available for testing"
STARTUP> sequence 380-400 *(To run only selected subtests)*
STARTUP> run
info: "mem4000 subtest 380 running"
+++>
<Thu Mar 26 12:52:30 1992> mem4000:../error_log.c:266
SW Info (DiagIN230): Test complete

Test: mem4000 R1.0 Subtest: 380 R1.0 Class: 4
Purpose: Memory testing via Memory Test Logic: address pattern.

***** SUBTEST SUCCESSFULLY COMPLETED *****
****
info: "mem4000 subtest 385 running"
Testing with pattern = 00000000 00000000, op = HOLD
Testing with pattern = ffffffff ffffffff, op = HOLD
Testing with pattern = a5a5a5a5 a5a5a5a5, op = HOLD
Testing with pattern = 5a5a5a5a 5a5a5a5a, op = HOLD
Testing with pattern = 69696969 69696969, op = HOLD
Testing with pattern = 96969696 96969696, op = HOLD
Testing with pattern = c3c3c3c3 c3c3c3c3, op = HOLD
Testing with pattern = 3c3c3c3c 3c3c3c3c, op = HOLD
Testing with pattern = 00000001 00000001, op = LEFT SHIFT
Testing with pattern = fffffffe fffffffe, op = LEFT SHIFT
```

.....continued on next page.....

```
Testing with pattern = 11111111 11111111, op = LEFT SHIFT
Testing with pattern = eeeeeeee eeeeeeee, op = LEFT SHIFT
Testing with pattern = ffffffff ffffffff, op = COMPLEMENT
Testing with pattern = a5a5a5a5 a5a5a5a5, op = COMPLEMENT
Testing with pattern = c3c3c3c3 c3c3c3c3, op = COMPLEMENT
Testing with pattern = 96969696 96969696, op = COMPLEMENT
Testing with pattern = 0fffffff 0fffffff, op = HOLD

+++>
<Thu Mar 26 12:54:13 1992> mem4000:../error_log.c:266
SW Info (DiagIN230): Test complete

Test: mem4000 R1.0 Subtest: 385 R1.0 Class: 4
Purpose: Memory testing via Memory Test Logic: various patterns.

***** SUBTEST SUCCESSFULLY COMPLETED *****
****
info: "mem4000 subtest 400 running"
Testing with pattern = 00000000 ffffffff
Testing with pattern = ffffffff 00000000
Testing with pattern = 55555555 00000028
Testing with pattern = 0bbbbbbb cccccccc
Testing with pattern = 33333333 0f0f0f0f
^CPRE-CLEANUP> exit

+++>
<Thu Mar 26 12:56:01 1992> mem4000:../../CTIsequencer.c:469
Test End (DiagER316): CTI Test Summary

test name: mem4000
runtime: 3:22.238
subtests started: 3 subtests passed: 2
subtests failed: 0
****

+++>
<Thu Mar 26 12:56:02 1992> mem4000:../../CTIutil.c:229
Test End (DiagER300): Test Termination Event
```

.....continued on next page.....

```
test name: mem4000
status: PASSED
****
spu>
```

---

3. An example of spu4000, st_810 only.

```
spu> spu4000

+++>
<Thu Mar 26 12:35:48 1992> spu4000:../../cti.c:242
Test Start (DiagER299): Test Startup Event

test name: spu4000
cwd: /users/diaguser
cmdline: spu4000
STARTUP> com *(Displays available commands)*
- - "!" "passes a quoted string to the shell"
- - "abort" "aborts a subtest if in "interrupt" or "run" state,
     otherwise aborts the test altogether"
- - "base" "sets the default output radix - 2, 8, 10, or 16
- - "changed" "[filename] print the changed parameters and their
     values in order changed"
- - "class" "[class] omit class to see all classes supply class to
     see info on that class and all of its subtests"
- - "com" "[name] show the help string for a command or parameter"
- - "cont" "runs the subtest sequencer"
- - "dep" "[first-last] show the subtests, omit the range for all"
- - "exit" "cleanup, then exit"
- - "get_par" "read in a set of parameters from the supplied
     filename"
- - "globals" "show parameters that have the CTI_GLOBALS flag set"
- - "help" "tells how to find information"
- - "log_file" "specifies a file for message logging"
- - "map" "map the specified window to the ctix display"
- - "par" "[par_name] show the parameters and their values"
- - "quit" "cleanup, then exit"
- - "rerun" "runs the sequencer starting with previous subtest"
- - "reset" "resets the CTI, sequencer, counters, & status "
- - "run" "specify a subtest sequence and restart sequencer"
```

.....continued on next page.....

```
- - "save" "[filename] save changed parameter values to the file."
- - "save_all" "[filename] save all parameter values to the file."
- - "skip" "skip n subtests in the sequence"
- - "status" "request a status update"
- - "sub" "[first-last] show the subtests in the run list, omit the
     range for all"
- - "sub_all" "[first-last] show the known subtests, omit the range
     for all"
- - "summary" "write parameters that have the CTI_SUMMARY flag
     set."
- - "test_par" "show parameters that are specific to the test"
- - "update_selects" "Select each installed board"
STARTUP> sequence 810 (To startup on st_810)*********
STARTUP> update_selects (Ensures all installed boards are
         tested)******
STARTUP> run
info: "spu4000 subtest 810 running"
Running Scalar Processor 6 to Crossbar Connectivity Test.
Running Scalar Processor 7 to Crossbar Connectivity Test.
Running Crossbar to Scalar Processor 6 Connectivity Test.
Running Crossbar to Scalar Processor 7 Connectivity Test.
Running Scalar/Vector Processor 6 Connectivity Test.
Running Scalar/Vector Processor 7 Connectivity Test.
Running Vector/Scalar Processor 6 Connectivity Test.
Running Vector/Scalar Processor 7 Connectivity Test.
Running Memory Board 6 to Crossbar Connectivity Test.
Running Memory Board 7 to Crossbar Connectivity Test.
Running Crossbar to Memory Board 6 Connectivity Test.
Running Crossbar to Memory Board 7 Connectivity Test.
Running Interface Adapter 8 to Crossbar Connectivity Test.
Running Crossbar to Interface Adapter 8 Connectivity Test.
Running NCU to Crossbar Connectivity Test.
Running Crossbar to NCU Connectivity Test.

+++>
<Thu Mar 26 12:39:14 1992> spu4000:../../CTIsequencer.c:469
Test End (DiagER316): CTI Test Summary
```

.....continued on next page.....

```
test name: spu4000
runtime: 1:19.035
subtests started: 1
subtests passed: 1
subtests failed: 0
****
COMPLETE> exit

+++>
<Thu Mar 26 12:40:30 1992> spu4000:../../CTIutil.c:229
Test End (DiagER300): Test Termination Event

test name: spu4000
status: PASSED
****

spu> spu4000

+++>
<Thu Mar 26 12:40:48 1992> spu4000:../../cti.c:242
Test Start (DiagER299): Test Startup Event

test name: spu4000
cwd: /users/diaguser
cmdline: spu4000
****
```

Jerry

3.18.2 Cache Controller Error Trouble Shooting

Recently, we have begun to experience more "Cache Controller Errors". As a result of this, I thought that I would attempt to explain what goes on and suggest the quickest response for resolving these pesky errors.

First off the cache controller error will generally occur during the boot process and a reboot will clear the error and allow the system to come up. Unfortunately this error will reappear the next time the system is booted.

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The Cache Controller Error indicates that a controller on the bus, either VME or Mbus, has issued a request, but the controller does not release the bus so that the CCU can status for the controller making the request. After making several attempts and determining the bus is indeed hung, the CCU will issue the "Cache Controller Error". By rebooting, the bus is cleared and the offending controller is reset in the process and so will allow the bus to free.

The only sure solution to troubleshooting this problem is to remove all controllers and reinstall one at a time until the defective controller is found. This is a tough way to go, but as the bus is hung, nothing else will be very successful. In some cases ccuadb can be of use to find an interrupt used by an active controller.

This problem will generally occur after powering the system off, or rebooting after a crash, but can occur during normal operation at multiuser.

Al,

3.18.3 ddb Utility Addendum

In the technical bulletin v3w17 there is a discussion of the utility ddb. This discussion included some examples. This should be considered an addendum to that technical bulletin.

First of all, it should be understood that ddb can only be used to execute cpu diagnostics and cannot be used for spu4000, mem4000 and cu4000. These diagnostics can only be executed under dsh. This will be discussed thoroughly in a future tech bulletin.

The examples in the previous tech bulletin makes the following recommendations:

```
vl_count/=w 10
Forced_faults/=w 1
Chain_mode/=w 1
```

These parameter entries will work just fine, but set the parameters for only one head at a time. The following entries will set these parameters for all heads under test and, by the way, are parameter entries listed under "status".

```
$vl_count 10
$data_ffaults 1 and/or $ip_ffaults 1
$chain_mode 1
```

.....continued on next page.....

It should be noted that all switches displayed by $status function correctly and should be used when changing any parameters. As can be seen all of the switches, except vl_count, are binary and can be tuned off with 0 and turned on with a 1.

It is also possible to run heads in parallel under ddb by the following method:

$parallel_mode 1

An additional benefit of using these switches is that their status can be monitored through $status.

It is also possible to execute individual subtests under ddb by using the following command:

[DDB] st_xx:r where xx equals the subtest to be executed and r indicates a run command.

This should be done with caution as some subtests require status and data generated in previous subtests and so failures could be misleading.

When executing diags under ddb a pass/fail message is not generated at the completion of the diags. The result will be a dump of register a1. If the contents of a1 is 0x100 then the diagnostic ran successfully. If the contents of a1 is anything other than 0x100 then the diagnostic failed.

Al,

3.18.4 Change in C3800 Hard Crashes

As many of you have already noticed the type of hard crashes being seen on C3800's has begun to change recently. This appears primarily due to the fact that the purge ram problems are being brought under control and there is opportunity for a new situation to present itself.

The new hard errors that are being seen a great deal are referred to as "NVRF1" and "NVRF2". The "NVRF1" crash is the more conventional error and presents with multiple gate arrays reporting parity errors from the Vector Unit. These reporting components will generally consist of members of the add pipe, or multiply pipe and can include all functional units. This will result in a list of from 5 to 16 hard errors on the same vector processor. It is also possible for a parity error to be indicated in an NVRF register, or not. A parity error will appear as an * by the NVRF that had the error.

An example of this type of error can be seen below:

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```
+++>
<Sat Apr 25 15:37:58 1992> /diag/bin/hard_logger.exc:../hard.c:125
SW Error (DiagER368): Hard Error Register Contents

detected_harderrors[0]= 00000100  detected_harderrors[1]= 00000041
enabled_harderrors[0]=  00005fff  enabled_harderrors[1]=  0000007f

Hard error Summary
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------     ----------      ---------     ---------
    0           VP_TYPE             2         nmisc_m.ybus_par_err
===================================================================

vp2:nmisc_m.ybus_par_err = 1
    Parity error script for ybus received by NMISC_M gate array.
  Register name              Ring value          Board signal name
-------------------------------------------------------------------
ybus_data<63:0>    00 00 00 00 02 00 00 00      M3_OP0_DAT<63..0>
ybus_par<0:7>       1  1  1  1  1* 1  1  1      M3_OP0_PAR<0..7>
* indicates parity error
       Ring   Nibble      Driving board signal
NVRF#  value  Parity  M3_OP0_DAT M3_OP0_NIBBLE_PAR
-------------------------------------------------------------------
NVRF0  0      1       <63..60>     <0>
NVRF2  0      1       <55..52>     <1>
NVRF4  0      1       <47..44>     <2>
NVRF6  0      1       <39..36>     <3>
NVRF0  0      1       <31..28>     <4>
NVRF2  0      1       <23..20>     <5>
NVRF4  0      1       <15..12>     <6>
NVRF6  0      1         <7..4>     <7>
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------     ----------      ---------     ---------
    1           VP_TYPE             2         nfad_m.ybus_par_err
===================================================================
```

.....continued on next page.....

```
vp2:nfad_m.ybus_par_err = 1
    Parity error script for ybus received by NFAD_M gate array.
  Register name              Ring value          Board signal name
-------------------------------------------------------------------
ybus_data<63:0>     00 00 00 00 02 00 00 00       M3_OP0_DAT<63..0>
ybus_par<0:7>        1  1  1  1  1* 1  1  1       M3_OP0_PAR<0..7>
* indicates parity error
       Ring    Nibble       Driving board signal
NVRF#  value   Parity   M3_OP0_DAT M3_OP0_NIBBLE_PAR
-------------------------------------------------------------------
NVRF0  0       1         <63..60>     <0>
NVRF2  0       1         <55..52>     <1>
NVRF4  0       1         <47..44>     <2>
NVRF6  0       1         <39..36>     <3>
NVRF0  0       1         <31..28>     <4>
NVRF2  0       1         <23..20>     <5>
NVRF4  0       1         <15..12>     <6>
NVRF6  0       1           <7..4>     <7>
-------------------------------------------------------------------
HARDERROR #      BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------      ----------      ---------     ---------
    2            VP_TYPE            2          nmul1.ybus_par_err
===================================================================
vp2:nmul[1].ybus_par_err = 1
    Parity error script for ybus received by NMUL[1] gate array.
  Register name              Ring value          Board signal name
-------------------------------------------------------------------
ybus_data<63:0>     00 00 00 00 02 00 00 00       M3_OP0_DAT<63..0>
ybus_par<0:7>        1  1  1  1  1* 1  1  1       M3_OP0_PAR<0..7>
* indicates parity error
       Ring    Nibble       Driving board signal
NVRF#  value   Parity   M3_OP0_DAT M3_OP0_NIBBLE_PAR
-------------------------------------------------------------------
NVRF0  0       1         <63..60>     <0>
NVRF2  0       1         <55..52>     <1>
NVRF4  0       1         <47..44>     <2>
NVRF6  0       1         <39..36>     <3>
```

.....continued on next page.....

```
NVRF0   0       1         <31..28>      <4>
NVRF2   0       1         <23..20>      <5>
NVRF4   0       1         <15..12>      <6>
NVRF6   0       1           <7..4>      <7>

-----------------------------------------------------------------
HARDERROR #      BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------      ----------      ---------     ---------
    3            VP_TYPE            2          nmul0.ybus_par_err
=================================================================
vp2:nmul[0].ybus_par_err = 1
    Parity error script for ybus received by NMUL[0] gate array.
  Register name              Ring value           Board signal name
-----------------------------------------------------------------
ybus_data<63:0>    00 00 00 00 02 00 00 00       M3_OP0_DAT<63..0>
ybus_par<0:7>       1  1  1  1  1* 1  1  1       M3_OP0_PAR<0..7>
* indicates parity error
       Ring   Nibble       Driving board signal
NVRF#  value  Parity  M3_OP0_DAT M3_OP0_NIBBLE_PAR
-----------------------------------------------------------------
NVRF0   0       1         <63..60>      <0>
NVRF2   0       1         <55..52>      <1>
NVRF4   0       1         <47..44>      <2>
NVRF6   0       1         <39..36>      <3>
NVRF0   0       1         <31..28>      <4>
NVRF2   0       1         <23..20>      <5>
NVRF4   0       1         <15..12>      <6>
NVRF6   0       1           <7..4>      <7>
```

The second error, referred to as NVRF2 appears as a slightly different fault. The reason it is referred to as NVRF2 is because it is currently believed that this error is actually caused by the same event that generates the NVRF1 failure. The difference being that the data has moved down the line some and is actually picked up on the NSP and is displayed as a VX_DATA parity error.

Little is currently understood with this failure, but with the release of v1.1.2 of the diagnostics more should become quickly known.

An output display of this error follows:

.....continued on next page.....

```
================================================================
[SPU @09:39:12] <Mon Apr 27 1992>

<Mon Apr 27 12:38:13 1992> /diag/bin/hard_logger.exc:../hard.c:125
SW Error (DiagER368): Hard Error Register Contents

detected_harderrors[0]= 02000000  detected_harderrors[1]= 00000041
enabled_harderrors[0]=  3f005000  enabled_harderrors[1]=  0000007f
****
Extractor Name: xrt.rtn_par_err_sp6
Port: 0
----------------------------------------------------------------
HARDERROR #      BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------      ----------      ---------     ---------
    0             SP_TYPE            3         ndp.yuvc_vx_err
================================================================
sp6:ndp0.yuvc_par_err = 2 \
sp6:ndp1.yuvc_par_err = 2 | These should all have the same value
sp6:ndp2.yuvc_par_err = 2 /
  Parity error script for Vx bus received by NDP0, NDP1, and NDP2
  gate arrays.
Register name     Ring value                     Board signal name
----------------------------------------------------------------
vx<>            00 00 00 00 00 04 00 00          VX_DATA<63..0>
vx<>            1  1  1  1  1  1* 1  1           VX_PAR<0..7>
* indicates parity error

----------------------------------------------------------------
HARDERROR #      BOARD TYPE      PORT/SIDE     EXTRACTOR
-----------      ----------      ---------     ---------
    1             SP_TYPE            3         nrc.sal_miss3_stop_in
================================================================
sp6:nrc0.par_err_stop_in = 1 \
sp6:nrc1.par_err_stop_in = 1 | These should all have the same value
sp6:nrc2.par_err_stop_in = 1 /

Parity error script for sal_miss1 bus received by NRC0, NRC1, and
NRC2 gate arrays.
```

.....continued on next page.....

```
Register name      Ring value              Board signal name
-------------------------------------------------------------------
sa1_miss3<>    0f 2d 33 48          SA1_MISS1<31..3>:SA1_ADDR2<2..0>
sa1_miss3<>     1  1  1  0*         SA1_ADDR2_PAR<0..3>
===================================================================
```

Al,

3.18.5 FDDI VIOP Window Usage

The numbers of windows and local pages used in the viop side of the fddi drivers are

```
number of windows :      29
number of local pages :   7
```

They are calculated as follows

usage	number of windows	number of pages
segments for command and status	2	2
request entries and mibs	0	1
recv buffer list	1	1
receiving packet	2 * 4 = 8	0
xmitting packet	2 * 8 = 16	0
trace buffers	0	2 + 1 = 3

....continued on next page.....

status polled by JP	2	0
total---->	29	7

Al,

3.18.6 Hard Error Interrogator Problem with V1.1 of Diagnostics

For all those that have chosen to load the new hard error interrogators after loading v1.1 of the diagnostics; It has been discovered that the new interrogators will not work with v1.1. For those that have loaded the interrogators prior to loading v1.1 of the diagnostics; The reload has replaced the interrogators with new ones that will function, but still not work the way that is desired. The interrogators referred to are the sp and vp interrogators.

Today, a new diagnostic tape, v1.1.2, will be released and this will include current patches as well as the proper interrogators. This new tape will be a complete release of diagnostics.

If you have not yet loaded v1.1 of the diagnostics, it is recommended that you wait for v1.1.2.

The patches included with this release will address HiPPI support and correct a problem where the clocks are restarting during errintd. This failure has interfered with proper analysis of previous failures.

Al,

3.18.7 cpu4233 Test Failure

cpu4233 subtest 401 will fail when mcm1 memory boards are installed. It runs correctly with mcm3 memory boards. These failures are seen when using Diagnostic Database/System Diagnostics rev 1.0 and I/O Diagnostics 5.0.

Thanks to Jim Whitmire for this input

* Dave Muir *

3.19.1 New CPU Diagnostic and I/O Diagnostic Tapes

Since the release of separate I/O and CPU diagnostic tapes, there is a change in how the /mnt/usr/lib/DB_cop is created. The cpu diag/ddb tape contains the file DB_cop_proc and the I/O diagnostic tape contains the file DB_cop_io. These two files are merged during 'installsw' to create DB_cop.

It is important to install the new CPU diag and I/O diag tape together. If the CPU diagnostic tape is installed without installing the IO diagnostics, the system will not boot since no IOP's will exist in the DB_cop file.

To determine the version of the diagnostics on a system, look at /mnt/PROCDIAG_REV and /mnt/IODIAG_REV on the SPU. If either of these files does not exist, then both the diags have not been installed

```
spu -r /mnt/PROCDIAG_REV
Copyright 1992 CONVEX Computer Corp.
All rights are reserved.
CREATED ON Mon Feb 10 14:22:43 1992
Product:        C3400/5500 System Diagnostics and Database, Version: V1.1
Release date:   February 12, 1992
Directories:    /mnt/bin, /mnt/test, /mnt/usr, /hw/cputest

spu -r /mnt/IODIAG_REV
Copyright 1992 CONVEX Computer Corp.
All rights are reserved.
CREATED ON Mon Feb 10 15:44:11 1992
Product:        CONVEX C200/C3200/C3400 I/O Diagnostics V1.0
Release date:   Feb 06, 1992
Directories:    /mnt/bin, /mnt/bin/lib, /mnt/test, /mnt/test/script,
                /mnt/usr, /mnt/usr/lib, /mnt/usr/scn, /mnt/man
```

* Dave Muir *

3.20.1 C3800 sst.log

C3800 systems being shipped this quarter (Q2) will contain a sst.log file in the /sst directory. This file contains the result of sst that was run on the system prior to final shutdown.

Jerry

3.20.2 C3800 Failure Analysis

It has frequently been asked how to proceed with analysis of different failures. While this is a very difficult question to answer there are some basic guidelines in existence for this purpose. Below is listed rules that have been generated for use with CXTS. These analysis rules are to aid in the decision process for determination of troubleshooting paths. The rules are for the NCU, NSP, NIA and NVP.

These rules are only guidelines and displayed here for information purposes, so that FE's can become more familiar with the analysis and extractor processes.

Extractor Name.	Rule.
cu_lckb_par_err	These error conditions are totally isolated to the
cu_ram_par_err	CU and will not involve any other component of the system.
cu_trp_harderr	This error has been disabled by scan. Checked to verify the scan ring of the CU, by running spu4000 subtest 611. If this passes then there is some software that is not initializing the board correctly.
cu_wr_dat_par_err	This error is on bad write data from the XS1O bits <23..0>. If this error is seen then there should also be a cu_ndat0_harderr. If there is a cu_ndat0_harderr then Check to see if there are any mb_iso_data_perr. If there are, and there is bad data in the xbar and the memory board, the problem may involve the port identified by the MB. All receivers (in this case the CU is a receiver) could be detecting the error. Indicates a potential connectivity problem. Run cpu4332 from a processor that is not the one indicated by the mb_iso_data_perr. This will verify that there is basic connectivity at speed

.....continued on next page.....

and spu4000 subtest 810 will probably not find anything. If this passes then run the test again from the processor that mb_iso_data_perr has identified. If this passes, the problem could still be connectivity. It would be time for the meter. Check the value of the terminations at the CPU backplane for the three lower byte of the write data.

cu_ndat1_harderr

Check to see if there are any mb_ise_data_perr. If there are, and there is bad data in the xbar and the memory board, the problem may be coming from the port which the MB has identified. All receivers (the CU is a receiver) could be detecting the error. Indicates a potential connectivity problem.

Run cpu4332 from a processor that is not the one indicated by the mb_ise_data_perr. This will verify that there is basic connectivity at speed and spu4000 subtest 810 will probably not find anything. If this passes then run the test again from the processor that mb_ise_data_perr has identified. If this passes, the problem could still be connectivity. It would be time for the meter. Check the value of the terminations at the CPU backplane for all the write data bits.

cu_ndat0_harderr

If this error is received there is no cu_wr_dat_par_err THEN the problem is likely to be on the most significant byte of the data. (bits <31..24>). Use the same rules as above.

Check to see if there are any mb_ise_data_perr. If there are, and there is bad data in the xbar and the memory board, the problem may be coming from the port which the MB has identified.

1) Run cpu4332 from a processor that is not the one indicated by the mb_ise_data_perr. This will verify that there is basic connectivity to the CU at speed and spu4000 subtest 810 will probably not find anything.

2) If this passes then run the test again from the processor that mb_ise_data_perr has identified.

3) IF this passes, the problem could still be connectivity. It would be time for the meter. Check the value of the terminations at the CPU backplane for the most significant byte of the write data.

4) IF cpu4332 fails at 1) then this failure would have to be diagnosed separately.

.....continued on next page.....

5) If the failure was another cu_ndat0_harderr then the connectivity between the CU and the XBAR should be examined on bits <31..24> from the xbar at the IO backplane.

6) If the connectivity is found to be good in 5) then switch the XS1 even and odd boards.

7) If the problem stays on the same side then pick the NCU or the Augat to replace.

NOTE The ndat gate arrays do not follow conventional naming conventions, as ndat1 is even and ndat0 is odd.

cu_addr_par_err_3_2
cu_addr_par_err_1
cu_addr_par_err_0

The Rules for these will be the same. The difference is in the actual bits involved with detecting the error. The same rules apply to the address that is applied to the data. That is the cpu4332 test. If the data in the xbar does not match the data in the board then the problem is the connectivity at the CU - XBAR interface. If there were mb_iso_addr_perr then the processor is probably the source of the problem. If the diagnostics do run and without error the next thing would be to meter the bits on the byte that was flagged as the error. (_0, _1, _3_2). If these were found to be normal impedance (52-54 ohms) then the next step would be to switch the XS0 even and odd boards and see if the problem moved sides.

NIA rules

```
#************ NIA harderror extractor list ******************
#
# I - should be internal
# F - should be internal, but might fall through from external
# X - could be external
# There are also some internals which might fall through to other internals,
# but those cases are handled by hord_logger extractor rules.
#
# The notation 'if ( extractor )' is true when the extractor reports an
# error.
# The notation 'extractor.word' refers to a value passed by the extractor
# in the event report.
```

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```
#
ia_xds_hdr_pe       I  XDS arrays detected a header parity error.
                       : reject NIA
ia_xds_wde_pe       I  XDS arrays detected even side write data parity error on data from
                       WDQ.
                       : reject NIA
ia_xds_wdo_pe       I  XDS arrays detected odd side write data parity error on data from WDQ.
                       : reject NIA
ia_cds_rd_pe        F  CDS arrays detected read data parity error on data from RDQ.
                       : if ( ia_rdq_wrt_pe )
                       :   { ignore this error }
                       : else
                       :   { reject NIA }
ia_rdq_wrt_pe       F  Parity error detected on write data during write access to RDQ.
                       : if ( ia_rdq_wrt_pe )
                       :   { ignore this error }
                       : else
                       :   { reject NIA }
ia_wdq_wrt_pe       I  Parity error detected on write data during write access to WDQ.
                       : reject NIA
ia_pi_hard_error    X  Pbus interrupt state machine hard error. CCU unexpectedly dropped its
                       interrupt request.
                       : /* start at 50% connection, 25% ccu, 25% nia *
                       : Ccu = ia_pi_hard_error.ccu
                       : if ( Ccu not installed ) { reject NIA }
                       : else
                       :   {
                       :   /* start at 50% connection, 25% ccu, 25% nia */
                       :   run sst on nia
                       :   run ccu_con on Ccu
                       :   }
ia_nxi_hard_error   X  NXI interrupt state machine hard error. XIOP unexpectedly dropped its
                       interrupt request.
                       : Xiop = ia_nxi_hard_error.xiop
                       : if ( Xiop > 1 ) { reject NIA } /* bad error report */
                       : else if ( Xiop not installed ) { reject NIA }
                       :         /* ia8 xiop0 is SPU */
                       : else
                       :   {
                       :    /* start at 50% connection, 25% xiop, 25% nia */
                       :    run sst on nia
```

```
                        :    run nxp.newcon on Xiop
                        :    }
ia_wdq_fflag_pe     I   WDQ flush flag parity error.
                        : reject NIA
ia_rdq_flag_pe      I   RDQ read error flag parity error.
                        : reject NIA
ia_rd_par_err_e     X   Parity error on read data from even side crossbar.
                        : Port = ia_rd_par_err_e.port
                        : if ( any other errors reported by even side xbar )
                        : { ignore this error }
                        : else if ( nia rtn_par_err stops xbar )
                        : /* if ( xrte:p_config & (1<<ia_rd_par_err_e.port))*/
                        : {
                        : if ( ias$Port:r_rdata_e == xrte:_look_aside_
                        : && ias$Port:r_rpar_e_s1_3_0 == xrte:_look_aside_ )
                        : { }
                        : }
                        : else /* data not stored on xbar for comparison */
                        : {
                        : run sys_con for the NIA
                        :
                        : }
ia_rd_par_err_o     X   Parity error on read data from odd side crossbar.
                        : Just like even side.

NSP rules

######
######   XBAR CASE
######

if extractor (nrc.xre_stop_in | nrc.xro_stop_in) then
  if nrc.xre_stop_in then
    check (xrt.rtn_par_err_sp? 0) for error
      if there is a failure on the xrte, follow it's rules to determine source of error.
      if no error exists on xrte then failure is either connectivity, a bad xrt, or a bad nsp
  try spu4000 -s 812 (to test connectivity)
    if no failure is found by spu4000 -s 812 then try swapping xtre-xtro, and reboot looking for
      failure to move, if it does then it's a bad xrt, if it doesn't, then move the nsp between cpus
      and reboot looking for the failure to move, if it does it's a bad nsp, if not then there is a
      resistive open/short not detectable by spu4000.
```

.....continued on next page.....

else if nrc.xro_stop_in then
check (xrt.rtn_par_err_sp? 1) for error
if there is a failure on the xrto, follow it's rules to determine source of error.
if no error exists on xrto then failure is either connectivity, a bad xrt, or a bad nsp
try spu4000 -s 812 (to test connectivity)
if no failure is found by spu4000 -s 812 then try swapping xtre-xtro, and reboot looking for failure to move, if it does then it's a bad xrt, if it doesn't, then move the nsp between cpus and reboot looking for the failure to move, if it does it's a bad nsp, if not then there is a resistive open/short not detectable by spu4000.

note: in the case of a resistive open you will need to know what the data held on the xtre and the nsp are for each failure and check to determine if the same data/parity line is failing, in which case after board swaps are exhausted you can point to a data/parity net to check connectivity on.

if extractor (npsw.statq_hard_err) then
try spu4000 -s 812 and /diag/hw/cutest/xc_con p? (to test connectivity)
if no failure is found by either then you have a problem. :^) this failure can be caused by 2 conditions, 1 is entirely contained on the nsp, the other is caused by an extra pop of the cu-sp.stat_en which actually goes from the ncu to the xcl and from the xcl to the nsp. It could be any of the 3 boards or resistive open/short on either net. I would try moving the processor and see if it follows it, if it doesn't then try swapping either the xcl or ncu till the problem goes away or both board have been swapped, in which case it must be a resistive connectivity problem.

note: in most cases it is impossible to tell if the failure is the internal error or the ncu error, but in a select few cases it is, so we will have to decide on a way to communicate which if either it is.

if extractor (npsw.ucode_pulled_hard_err) then
this failure isn't really a hard error at all, it's more like a ConvexOS fatal error pulled by the microcode on the nsp. In most cases the failure is cased by one of the xrt boards stopping and bogus data being used for instruction cache data. Check for hard errors in the xbar, if there aren't any, then it could be just about any board in the system. Depending on the uir1_upc value. If need be we can decide on more specific rules but this is as far as I will go for now.

note: it may be nice if I pass the uir1_upc with this extractor, as it is about the only way to gain even a bit of insight into this failure.

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######
NVP CASE
######

if extractor (nag0.vxaq_par_err | nag1.vxaq_par_err) then
  check (vp?) for errors
    if there is a hard error on the nvp, then ignore the nsp errors for now unless the nvp rules end up pointing at the nsp.
    if no error exists on the nvp then failure is either connectivity, a bad nvp, or a bad nsp
    try spu4000 -s 812 (to test connectivity)
      if no failure is found by spu4000 -s 812 then try swapping nvp with another cpu (if possible), and reboot looking for failure to move, if it does then it's a bad nvp, if it doesn't, then move the nsp between cpus and reboot looking for the failure to move, if it does it's a bad nsp, if not then there is a resistive open/short not detectable by spu4000.
    If you only have 1 cpu then I would replace the nvp first and see if the failure goes away, if not replace the nvp and try the nsp. If the failure still persists then there is a resistive open/short not detectable by spu4000.

  note: in the case of a resistive open you will need to know what the data held on the nsp was for each failure and check to determine if the same data byte is failing, in which case after board swaps are exhausted you can at least narrow the nets to be checked for connectivity to 9.

if extractor (ndp.yuvc_vx_err) then
  check (vp?) for errors
    if there is a hard error on the nvp, then ignore the nsp errors for now unless the nvp rules end up pointing at the nsp.
    if no error exists on the nvp then failure is either connectivity, a bad nvp, or a bad nsp
    try spu4000 -s 812 (to test connectivity)
      if no failure is found by spu4000 -s 812 then try swapping nvp with another cpu (if possible), and reboot looking for failure to move, if it does then it's a bad nvp, if it doesn't, then move the nsp between cpus and reboot looking for the failure to move, if it does it's a bad nsp, if not then there is a resistive open/short not detectable by spu4000.
    If you only have 1 cpu then I would replace the nvp first and see if the failure goes away, if not replace the nvp and try the nsp. If the failure still persists then there is a resistive open/short not detectable by spu4000.

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note: in the case of a resistive open you will need to know what the data held on the nsp was for each failure and check to determine if the same data byte is failing, in which case after board swaps are exhausted you can at least narrow the nets to be checked for connectivity to 9.

######
ANY OTHER CASE
######

if any other extractor finds an error besides the ones listed above, then the error is entirely contained on the nsp and the board should be rejected.

NVP rules

######
NSP CASE
######

if extractor (nis0.is_par_err | nis1.is_par_err) then
  check (sp?) for errors
    if there is a hard error on the nsp, then ignore the nvp errors for now unless the nsp rules end up pointing at the nvp.
    if no error exists on the nsp then failure is either connectivity, a bad nvp, or a bad nsp
    try spu4000 -s 812 (to test connectivity)
      if no failure is found by spu4000 -s 812 then try swapping nvp with another cpu (if possible), and reboot looking for failure to move, if it does then it's a bad nvp, if it doesn't, then move the nsp between cpus and reboot looking for the failure to move, if it does it's a bad nsp, if not then there is a resistive open/short not detectable by spu4000.
      If you only have 1 cpu then I would replace the nsp first and see if the failure goes away, if not replace the nsp and try the nvp. If the failure still persists then there is a resistive open/short not detectable by spu4000.

note: in the case of a resistive open you will need to know what the data held on the nvp was for each failure and check to determine if the same data byte is failing, in which case after board swaps are exhausted you can at least narrow the nets to be checked for connectivity to 9.

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######
ANY OTHER CASE
######

if any other extractor finds an error besides the ones listed above, then the error is entirely contained on the nvp and the board should be rejected.

Al,

3.20.3 C3800 SST Overview

This is a brief overview of sst as it pertains to the C3800. The only executable version of sst is currently v2.2.2. No lower version will execute properly. Additional information can be obtained from the SST Users Manual, part number 760-001530-001.

To install sst it is necessary to perform the following

1) cd /sst
2) load sst data tape
3) installsw -i

To execute sst tests it is necessary to cd /sst and enter "sst" at the spu prompt. This will display the Main Menu as shown below. At the "sst prompt" enter a "4". This will generate a response that asks for the pattern tape to be loaded. This is the same tape that is used to load the sst execution files. The program will then begin to pack patterns of rings that are executable on that particular system. Depending on the number of different part number boards installed, this process will take 20-60 minutes.

NOTE It is possible to pack these pattern and install sst with the system at multiuser.

At the completion of the packing phase, the user will be asked if they wish to execute the tests. If the system is booted it will be necessary to bring it to the spu before proceeding. Execution of the tests will take 6-9 minutes depending on the configuration of the system.

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SST Main Menu

1.	configure	configuration menu
2.	test	test parameter menu
3.	display	display parameter menu
4.	run	run an sst test for a set of patterns
5.	continue	continue an interrupted run
6.	retry	retry beginning at first failure
7.	save	save the current sst state
8.	restore	restore a previous sst state
9.	clean	delete all unusable image sets
10.	delete	delete an image set
11.	do	execute commands from a file
12.	help, ?	display help information
13.	quit	exit sst

sst >

Options 1-3 of the main menu are for display of additional menus:

The configuration menu is to be used to alter the hardware configuration to be tested. If a failure is encountered in any ring the only means to execute rings past that point is to exclude the failing ring. This can be accomplished from the configuration menu by entering "-e xx.0" at the sst prompt, where xx is the ring name.

Configuration Menu

1.	display		display the current configuration
2.	hardware,	-h	set configuration to installed hardware
3.	tape,	-t	set configuration to rings with networks on tape
4.	clear,	-c	clear the current configuration
5.	add,	-a	add scan rings associated with board
6.	remove,	-r	remove scan rings associated with board
7.	include,	-i	include rings
8.	exclude,	-e	do not include rings
9.	asm,	-m	force board assembly revision
10	wire,	-w	force board wire revision
11.	part,	-t	force board part number
12.	main		go to main menu

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The test parameter menu is used to display, or modify test parameters during the execution of sst. Display of submenus will not be listed hear as they are self explanatory and would serve only to waste text.

Test Parameter Menu

1.	display	display all current test parameters
2.	default	default all current test parameters
3.	pause	test pause submenu
4.	loop	test loop submenu
5.	limit	test limit submenu
6.	log	test log control submenu
7.	main	return to main menu

Below is the coverage provided by sst for the listed boards:

Table 1: SST Stuck-At Fault Coverage

Board	total stuck-at faults	single-board coverage (percentage)	single-board + cross-board scan coverage (percentage)	bits detected	faults
NVP	1,044,166	74.33%	74.86%	781,662	15,912
NSP	1,029,478	86.69%	87.58%	901,616	18,514
NIA	410,502	76.02%	90.10%	369,862	6,793
NCU	345,318	40.21%	43.46%	150,075	3,039
NMB	290,846	77.41%	79.22%	230,408	9,474
XS1	230,666	51.44%	98.86%	228,036	4,892
XS0	146,972	86.85%	88.34%	129,835	4,166
XRT	99,900	67.23%	85.77%	85,684	4,091
XCL	54,396	18.57%	21.37%	11,624	252

NOTES:

1) NMB coverage does not include NMC's. The NMC's are not covered by SST.

2) XCL coverage is low due to the fact that it is the scan engine. (theoretically it is covered implicitly by its use in testing the rest of the boards)

.....continued on next page.....

3) The Single-Board + Cross-Board Coverage Percentage for a given board, is the coverage for that board in the maximum populated configuration for the given machine. So, this number technically only applies to that configuration, but it can also be viewed from the standpoint that this number is possibly considering circuitry that is not being used in a less populated machine.

4) The 4th column numbers are the detected faults. These numbers can be used to generate a system coverage number. Just add up the appropriate numbers from column 1. Generate a sum of the appropriate numbers from column 4, and then divide the 2 summations into each other, and you get your system coverage number.

5) Coverage for a C3880 with 8 memory boards is 80.88%.

6) In general SST uses the longest single scan ring available on a given board. (In the case of the Javelin boards: MCM, MCM3 and PI2, we use the log rings in addition to the main ring, since there is not a scan configuration that lumps that ring into the main ring.)

Al,

3.20.4 C3800 Boot Scripts

It should be understood that there are two boot scripts for the C3800. The primary script is located in /mnt/os, on the SPU, and should be executed when in the CONVEX_OS screen under rmtdiag. The other script is located in /diag/bin.

The second boot script in /diag/bin is really a redirect from the spu window to the CONVEX_OS window. This one should be executed normally. The script appears below:

```
#! /bin/sh

if /diag/bin/sfp -k OFF; then
        echo "Key is in OFF position";
else
        echo 'Boot command sent to CONVEXOS CONSOLE window. Look there for output.'
        echo "cd /mnt/os; /mnt/os/boot $1" > /tmp/console_command;
        chmod 666 /tmp/console_command;
        kill_by_name CONVEXOS_CONSOLE -USR2;
fi
```

.....continued on next page.....

Executing the boot command from /mnt/os in the spu window means that this redirect to the OS window will not take place and so the boot will not function as planned.

It is, therefore, recommended that no boot be initiated under /mnt/os, or that the full path for the boot be used. In other words, initiate the boot process with /diag/bin/boot. This will avoid any unnecessary problems.

Al,

3.20.5 C3800 SPU "backup" and "restore"

"backup"

Edit "/etc/backup" and change "/dev/nrst1" to "/dev/nrst0".

To backup the SPU do the following:

1. Insert a write enabled DAT tape in the tape drive.
2. "su" to become root.
3. cd /
4. /etc/backup

This will dump all of the SPU file systems onto one tape.

The "/etc/backup" script looks at "/etc/fstab" to determine which file systems to dump. Here is what "fstab" looks like on a SPU running Diags 1.1.2:

```
/dev/sd0a / 4.2 rw 1 1
/dev/sd0e /mnt 4.2 rw 1 3
/dev/sd0f /diag 4.2 rw 1 3
/dev/sd0g /usr 4.2 rw 1 2
/dev/sd0h /sst 4.2 rw 1 3
```

"/etc/backup" would dump the file systems in the following order:

```
/
/mnt
/diag
/usr
/sst
```

.....continued on next page.....

Be sure to make note of the order the file systems are dumped, so you will have the proper info if you need to "restore" from the "backup" tape.

"restore"

The "/etc/restore" program is actually linked to "/usr/etc/restore".

If the "/" or "/usr" file systems are damaged, we must load SpuOS from scratch to recover the "/etc/restore" program. This procedure requires about 1.5 hours.

If the "/mnt", "/diag" or "/sst" file systems are damaged, they can be recovered from the "backup" tape.

Here is an example of a "/diag" and "/sst" restore from the "backup" created above:

1. Become root.
2. mount -vat 4.2 (mount all 4.2 type file systems listed in "/etc/fstab")
3. Insert "backup" tape into DAT drive.
4. mt rew
5. mt fsf 2 (space tape forward to /diag)
6. cd /diag
7. /etc/restore xv
8. mt rew
9. mt fsf 4 (space tape forward to /sst)
10. cd /sst
11. /etc/restore xv

NOTE: Depending on the type of file system damage, it might be faster to rebuild the complete disk from scratch than to use the "restore" program. Total time about 2.5 hours.

Dan Brenner

3.20.6 750mb Disk Module Jumpers

The following chart shows the jumper configuration for the 750mb disk module used in the RDS, C3400-ES internal disk and the QuadPack disk enclosure.

The unit number is selected by jumpers on JP213 on the component side of the drive control board.

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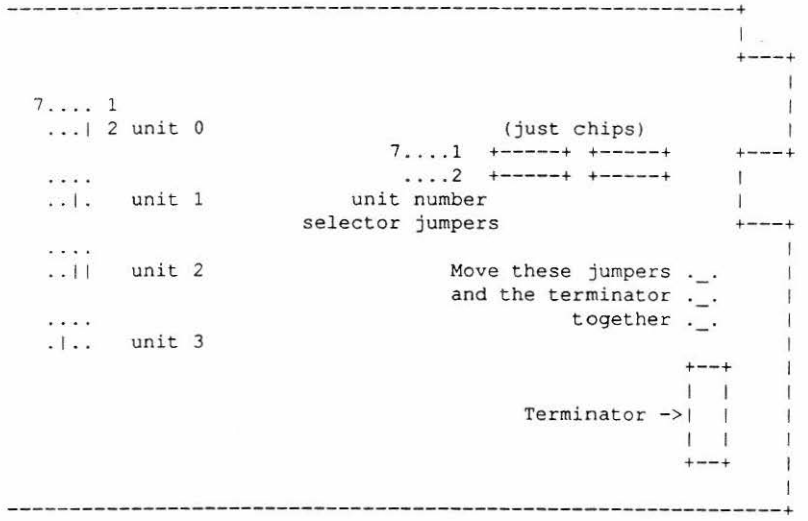
The terminator is placed on the last drive in the chain. If you move the terminator, you must also move the three jumpers located adjacent to the terminator



Kelvyn

3.20.7 C3400 Series SCM Error Codes

The following chart is for the C3400 series processors.

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JSM Error and Message Codes firmware revision 1.7

Code	Error/Message
00	Deadman timer indicates JSM internal problem
02	SP-SM.PWRINTAK* failure
04	SP-SM.SMBDATA<7..0>* failure
07	SP-SM.SPUDCOK failure
08	A/D Convertor Timed Out
0B	SP5 Illegal Instruction
0D	SP5 instruction cycle timed out
0F	Checksum failure on JSM
14	CPU7 installed incorrectly
15	CPU3 installed incorrectly
1A	CPU6 installed incorrectly
1B	CPU2 installed incorrectly
1C	SP5 installed incorrectly
1D	CUJ installed incorrectly
1E	ME0 installed incorrectly
1F	MO0 installed incorrectly
20	ME1 installed incorrectly
21	MO1 installed incorrectly
22	ME2 installed incorrectly
23	MO2 installed incorrectly
24	ME3 installed incorrectly
25	MO3 installed incorrectly
27	CPU1 installed incorrectly
28	CPU5 installed incorrectly
2D	CPU0 installed incorrectly
2E	CPU4 installed incorrectly
33	PIX installed incorrectly
34	PIY installed incorrectly
42	PS2 power supply temp failure
43	PS3 power supply temp failure
44	PS4 power supply temp failure
45	PS5 power supply temp failure
46	PS6 power supply temp failure
47	PS7 power supply temp failure
48	PS8 power supply temp failure

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JSM Error and Message Codes firmware revision 1.7

Code	Error/Message
61	PS1 AC power failure
62	PS2 AC power failure
63	PS3 AC power failure
64	PS4 AC power failure
65	PS5 AC power failure
66	PS6 AC power failure
67	PS7 AC power failure
68	PS8 AC power failure
69	HMU PS5 AC power failure (-4.5V) (Hot Mockup)
6A	HMU PS6 AC power failure (+5V) (Hot Mockup)
6B	HMU PS7 AC power failure (-2V) (Hot Mockup)
71	+5.0V DC power supply failure
72	+12.0V DC power supply failure
73	-12.0V DC power supply failure
74	-5.0V DC power supply failure
75	-4.5V DC power supply failure
76	-2.0V DC power supply failure
77	-5.2V DC power supply failure
78	HMU +5.0V DC power supply failure (Hot Mockup)
79	HMU -4.5V DC power supply failure (Hot Mockup)
7A	HMU -2.0V DC power supply failure (Hot Mockup)
82	PS2 current sharing failure
83	PS3 current sharing failure
84	PS4 current sharing failure
85	PS5 current sharing failure
86	PS6 current sharing failure
87	PS7 current sharing failure
88	PS8 current sharing failure
91	-4.5V current sharing out of tolerance
92	-2V current sharing out of tolerance
93	+5V current sharing out of tolerance

continued on next page.....

JSM Error and Message Codes firmware revision 1.7

Code	Error/Message
A0	Intake thermistor exceeds tolerance
A1	Exhaust thermistor exceeds tolerance
A2	PI2 terminator thermistor exceeds tolerance
A3	JSM thermistor exceeds tolerance
B1	CUJ airflow failure
B2	PIY airflow failure
B3	VME airflow failure (C3400-ES Only)
C0	Insufficient power supplies for configuration
E0	FN0 failure
E1	FN1 failure
E2	FN2 failure
E3	FN3 failure
E4	FN4 failure
E5	FN5 failure
E6	FN6 failure
E7	FN7 failure

* Dave Muir *

3.21.1 C2/C3200 Diag Failure with SecureOS

If you have loaded SecureOS on a C2/C3200 system, cpu4010 will fail class 7 subtests. You can execute the "secure off" command on the spu and cpu4010 will pass. You should then execute "secure on", on the spu, before running other diags or booting the system. If you DO NOT execute the "secure on" command, cpu4232 and 4233 will fail.

Thanks to Shawn Fuller for this input.

Dan Brenner

3.21.2 C3800 IA Soft Errors

It should be understood that IA soft errors, on a C3800, are the equivalent of PIA soft errors on the C2. In essence it means that the NIA has detected a hard error form one, or more CCU's. These errors can indicate anything from a failed CCU to a dropped data bit in a Pbus transfer.

Although it is possible for the NIA to cause this failure, it is not first choice. The CCU's should always be the primary suspect, followed by the devices on the CCU. In the cases of controllers causing the problem, the procedure would be the same as for the C2.

In order to isolate the failure there are two diagnostic tests that can be useful. These tests are pb_walk and idc_con. As idc_con will only run against an IDC, it may be necessary to move an IDC into the suspected slot.

The utility pb_walk can be executed against a specific Pbus by entering:

pb_walk x (where x is the Pbus to be tested)

In addition, it may be helpful to execute the test with "ignore errors" set so that all patterns can be tested. This will help in identifying any bit patterns that are unsuccessful. If this is not done then pb_walk will always stop execution after the first error. To accomplish this, execute the following:

pb_walk -e 0 1 ia8 (In this example, the test will be executed against Pbus's 0 and 1 on IA8 and will ignore the errors and run all patterns to completion)

Using the "-e" switch enables you to search for dropped, or shorted bits as the test runs through the sliding pattern. Individual net problems will become obvious very quickly.

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It may also be helpful to loop on the test and for this a script will have to be written. An example csh script is as follows:

```
#
while (1)
pb_walk -e 0 1
idc_con 32 34
end
```

The utility idc_con is included in this script as a further example. Keep in mind that this is a csh script and so, to execute will require popping a csh window on the OPUS, or enter a /bin/csh at the spu prompt.

As mentioned above idc_con can also be helpful for isolating these failures. The same "-e" switch can be used with idc_con. The CCU slot must be entered when executing idc_con, or it will not execute.

For the best chance at locating the source of the failure, it is best to execute these tests directly after a crash. It may be necessary to issue a cleanup if "clock generator busy" messages are encountered.

SST will be of no assistance in this area as there are no modules loaded for the TTL nets.

As mentioned in a previous Tech Bulletin, rslog can be very helpful in isolating the failure to a specific Pbus and , or CCU. Please see that info for more details.

Al,

3.21.3 C3800 SST Shortcuts

There are some shortcuts that can be taken when executing sst commands in a very specific troubleshooting effort. For example when executing modules for one specific component, the following command may be helpful:

```
sst conf -c -i ia8   (Where conf is the menu to be used, -c clears the previous config, -i
                      includes the ia8 for testing.)
```

This will cause the configuration to be cleared and include only the ia8 on the next run. This command will leave you in the configuration menu, so to execute, it will be necessary to quit to the main menu and issue the run command. Multiple menus can be entered from the same line by separating them by ";".

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Adaptations of this method can be very helpful when doing specific testing. When running SST on the entire configuration, this would be of little use.

Al,

3.21.4 C3800 I/O Minimum Revision Levels

Please remember, as indicated in a previous tech bulletin, the C3800 requires the minimum revision levels of the following:

VIOP	K
IDC	T
TLI	G

Al,

3.21.5 Format Error With idcfmtr

The idcfmt utility will occasional abort if it receives a "non-media related cmi code 0x1050 error from disk drive?". This will make the disk drive unusable with ConvexOs.

Version 5.0.2.0 of the IDC firmware has been released with a new version of idcfmtr which corrects this problem. If you have a customer who is having this problem, please contact the TAC. This release will not be shipped to all customers as a routine software distribution. It will be installed on all systems being shipped from Richardson, and will be included in the next release of IDC firmware.

3.21.6 INSTALL Scripts on C3400 systems

The INSTALL scripts will be on all systems shipped in the third quarter. Operation of these scripts are the same as versions shipped on the C2xx systems. However a new utility called 'sos' is being used to run the scripts.

To run the INSTALL script, change directories to mnt/cjxx/sos. Enter the command sos 'script-name'. All the applicable processor diagnostics will be run.

You must run the INSTALL script from the sos directory. A logfile of script execution is created in /mnt/cjxx/sos/logdir.

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The SYSTEMS script occasional reports an error "diag broken". This is normally caused by an sos bug. To insure that the script is at fault, run the "broken" diagnostic individually from dshell.

You can determine the test switches that are being used for the diagnostic looking at the INSTALL script. It is fairly evident from the script what options are being used.

I will send more information on sos in a later tech bulletin.

* Dave Muir *

3.22.1 There is no technical information for this week's bulletin.

* Dave Muir *

3.23.1 C3800 Hard Errors

The following is a list of all possible hard errors associated with the C3800:

MB_BOARD: mb_bcga_ise_cycle, mb_even_illegal_row_addr,
mb_bcga_ise_hi_addr, mb_ise_addr_perr,
mb_bcga_ise_low_addr, mb_ise_data_perr,
mb_bcga_ise_mid_addr, mb_ise_zone_perr,
mb_bcga_iso_cycle, mb_iso_addr_perr,
mb_bcga_iso_hi_addr, mb_iso_data_perr,
mb_bcga_iso_low_addr, mb_iso_zone_perr,
mb_bcga_iso_mid_addr, mb_odd_bank_ctl_err,
mb_even_bank_ctl_err, mb_odd_bank_cyc1_err,
mb_even_bank_cyc1_err, mb_odd_bank_cyc2_err,
mb_even_bank_cyc2_err, mb_odd_bank_cyc3_err,
mb_even_bank_cyc3_err, mb_odd_bank_perr,
mb_even_bank_perr, mb_odd_illegal_dram_addr,
mb_even_illegal_dram_addr, mb_odd_illegal_row_addr;

VP_BOARD: a_vm.uir_par_err, ndiv5.xbus_par_err, nmul0.xbus_par_err,
l_vm.uir_par_err, ndiv5.ybus_par_err, nmul0.ybus_par_err,
m_vm.uir_par_err, nfad_a.xbus_par_err, nmul1.xbus_par_err,
ndiv.xbus_par_err, nfad_a.ybus_par_err, nmul1.ybus_par_err,
ndiv.ybus_par_err, nfad_m.xbus_par_err, nmul2.xbus_par_err,
ndiv0.xbus_par_err, nfad_m.ybus_par_err, nmul2.ybus_par_err,
ndiv0.ybus_par_err, nib_par_err, nmul3.xbus_par_err,
ndiv1.xbus_par_err, nis0.is_par_err, nmul3.ybus_par_err
ndiv1.ybus_par_err, nis1.is_par_err, nvd.vd_par_err,
ndiv2.xbus_par_err, nmisc_a.xbus_par_err, nvp_hard_err,
ndiv2.ybus_par_err, nmisc_a.ybus_par_err, rslt_par_err,
ndiv3.xbus_par_err, nmisc_m.xbus_par_err,
ndiv3.ybus_par_err, nmisc_m.ybus_par_err,
ndiv4.xbus_par_err, nmul.xbus_par_err,
ndiv4.ybus_par_err, nmul.ybus_par_err;

SP_BOARD: dcd0_wr_par_err, nfad.xbus_par_err, nrc0.rctrl_par_err,
dcd1_wr_par_err, nfad.ybus_par_err, nrc1.edata_que_par_err,
dct0_wr_par_err, niad0.mxi_par_err, nrc1.odata_que_par_err,
dct1_wr_par_err, niad0.ybus_par_err, nrc1.rctrl_par_err,
dcu0_wr_par_err, nrc.xre_stop_in, nrc.xro_stop_in,

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niad1.mxi_par_err, nrc2.edata_que_par_err, dcu1_wr_par_err,
niad1.ybus_par_err, nrc2.odata_que_par_err, icd_wr_par_err,
nmisc.xbus_par_err, nrc2.rctrl_par_err, ict_wr_par_err,
nmisc.ybus_par_err, nrfa.extdata_par_err, lat_wr_par_err,
nmul.xbus_par_err, nrfa0.bbus_par_err, nag0.displ_par_err,
nmul.ybus_par_err, nrfa0.cbus_par_err, nag0.ixaq_par_err,
npa0.ctag_par_err, nrfa0.displ_par_err, nag0.uirl_par_err,
npa0.ctval_par_err, nrfa0.nrfa_wcs_par_err, nag0.updq_par_err,
npa0.cval_par_err, nrfa1.bbus_par_err, nag0.vxaq_par_err,
npa0.pdata_par_err, nrfa1.cbus_par_err, nag0.zbus_par_err,
npa0.ptag_par_err, nrfa1.displ_par_err, nag1.displ_par_err,
npa0.ptval_par_err, nrfa1.nrfa_wcs_par_err, nag1.ixaq_par_err,
npa0.pval_par_err, nrfa2.bbus_par_err, nag1.uirl_par_err,
npa1.ctag_par_err, nrfa2.cbus_par_err, nag1.updq_par_err,
npa1.ctval_par_err, nrfa2.displ_par_err, nag1.vxaq_par_err,
npa1.cval_par_err, nrfa2.nrfa_wcs_par_err, nag1.zbus_par_err,
npa1.pdata_par_err, nrfa3.bbus_par_err, ndc.uirl_par_err,
npa1.ptag_par_err, nrfa3.cbus_par_err, ndiv.xbus_par_err,
npa1.ptval_par_err, nrfa3.displ_par_err, ndiv.ybus_par_err,
npa1.pval_par_err, nrfa3.nrfa_wcs_par_err, ndp.yuvc_par_err,
npar.br_que_par_err, nsp_hard_error_script, ndp0.cupd_par_err,
npar.inst_tag_par_err, nus.nus_wcs_par_err, ndp0.pmod_par_err,
npar.inst_valid_par_err, nus.srv_rd_par_err, ndp0.pref_par_err,
npar.look_tag_par_err, pted0_wr_par_err, ndp1.cupd_par_err,
npar.look_valid_par_err, pted1_wr_par_err, ndp1.pmod_par_err,
npar.que_par_err, ptet0_wr_par_err, ndp1.pref_par_err,
npsw.npsw_wcs_par_err, ptet1_wr_par_err, ndp2.cupd_par_err,
nrc.par_err_stop_in, ndp2.pmod_par_err, nrc0.edata_que_par_err,
ndp2.pref_par_err, nrc0.odata_que_par_err, srd_wr_par_err,
nrc.eybus_stop_in, nrc.oybus_stop_in, nrc.sa1_miss3_stop_in,
npsw.statq_hard_err, npsw.ucode_pulled_hard_err;

IA_BOARD: ia_nxi_hard_error, ia_rdq_flag_pe, ia_xds_hdr_pe,
ia_pi_hard_error,
ia_rdq_wrt_pe, ia_xds_wde_pe, ia_rd_par_err_e, ia_wdq_fflag_pe,
ia_xds_wdo_pe, ia_cds_rd_pe, ia_rd_par_err_o, ia_wdq_wrt_pe;

CU_BOARD: cu_addr_par_err.0, cu_addr_par_err.1, cu_addr_par_err.3.2,
cu_lckb_par_err, cu_ndat0_harderr, cu_ndat1_harderr,
cu_ram_par_err, cu_trp_harderr, cu_wr_dat_par_err;

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XS0_BOARD: xs0.bad_send_par_err, xs0.lone_hard_err, xs0.pcm_err_a,
xs0.pcm_err_b, xs0.send_par_err_mb0, xs0.send_par_err_mb1,
xs0.send_par_err_mb2, xs0.send_par_err_mb3, xs0.send_par_err_mb4,
xs0.send_par_err_mb5, xs0.send_par_err_mb6, xs0.send_par_err_mb7,
xs0.send_par_err_ncu;

XS1_BOARD: xs1.bad_send_par_err, xs1.lone_hard_err, xs1.send_par_err_mb0,
xs1.send_par_err_mb1, xs1.send_par_err_mb2, xs1.send_par_err_mb3,
xs1.send_par_err_mb4, xs1.send_par_err_mb5, xs1.send_par_err_mb6,
xs1.send_par_err_mb7, xs1.send_par_err_ncu;

XRT_BOARD: rctl.bad_req_mb0, rctl.bad_req_mb1, rctl.bad_req_mb2,
rctl.bad_req_mb3, rctl.bad_req_mb4, rctl.bad_req_mb5,
rctl.bad_req_mb6, rctl.bad_req_mb7, rctl.bad_req_ncu,
rctl.cr_accel_err, rxbr0.overflow, rxbr0.underflow, rxbr1.overflow,
rxbr1.underflow, rxbr2.overflow, rxbr2.underflow, rxbr3.overflow,
rxbr3.underflow, rxbr4.overflow, rxbr4.underflow, xrt.bad_rd_rdy_mb0,
xrt.bad_rd_rdy_mb1, xrt.bad_rd_rdy_mb2, xrt.bad_rd_rdy_mb3,
xrt.bad_rd_rdy_mb4, xrt.bad_rd_rdy_mb5, xrt.bad_rd_rdy_mb6,
xrt.bad_rd_rdy_mb7, xrt.bad_rd_rdy_ncu, xrt.bubble_error,
xrt.no_rd_rdy_mb0, xrt.no_rd_rdy_mb1, xrt.no_rd_rdy_mb2,
xrt.no_rd_rdy_mb3, xrt.no_rd_rdy_mb4, xrt.no_rd_rdy_mb5,
xrt.no_rd_rdy_mb6, xrt.no_rd_rdy_mb7, xrt.no_rd_rdy_ncu,
xrt.rtn_par_err_nia, xrt.rtn_par_err_sp0, xrt.rtn_par_err_sp1,
xrt.rtn_par_err_sp2, xrt.rtn_par_err_sp3, xrt.rtn_par_err_sp4,
xrt.rtn_par_err_sp5, xrt.rtn_par_err_sp6, xrt.rtn_par_err_sp7;

Al,

3.23.2 Version 2.0 of C3800 Diagnostics

With the release of version 2.0 of the C3800 diagnostics there are some enhancements and fixes that all FE's should know about. The differences from v1.1.2 of the diags are detailed as follow. Most important changes will be denoted with *:

1) Will light the screen when a hard error is encountered. This will prevent system failures from being missed due to the screen blank mechanism.

* 2) Hard_logger has been modified to dump more information on the occurrence of NVRF failures.

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3) The utility modem_init has been modified to fix problems with modem initialization.

4) Modified to configure the net in accordance with the presence of SECURE Mode. If SECURE is running then the net will be disabled.

* 5) The us microcode includes intrinsic instruction fixes and real time operation modifications.

6) The sr ucode is modified for real time operation.

* 7) The file /diag/db/modem_parms is modified to fix modem initialization problems.

8) The vttga and vtt busses on the XBAR are skewed the same as other boards installed in the system.

* 9) The modem_init utility is removed from rc.local, so as not to interfere with changes made to activate non standard modems.

** 10) Contains a fix for the intermittent "async memory error" panics that have plagued the OPUS.

HINT In case you are on site without release notes, the install command for loading diags is:

/etc/installsw -i 2>&1 | tee /tmp/installsw.log

Al,

3.23.3 Checking Nets With a Fluke Meter

It should be kept in mind that the fluke meters and most others, that are used in the field, have an auto-range function. Activation of this function is generally indicated by a small bullseye display.

It is recommended that this function not be used when looking for net connectivity problems on C family backplanes. The auto-range function will greatly slow the reaction of the meter display and thus lead to erroneous measurements. In many cases the readings will be as much as 2 ohms higher than the actual resistance. These differences will lead to findings that are not compatible with sound troubleshooting decisions.

In cases where the difference between a good and bad net is less than 1/2 ohm, a 2 ohm difference can cause problems. Please bear this in mind when buzzing backplanes.

Al,

3.23.4 C3800 mminit

It should be understood that the mminit process, on the C3800, is accomplished by the Memory Test Logic (MTL), located on the NCU, and does not involve the heads in any way. Therefore, it is not possible to redirect this function to a head, or I/O, as was possible on other C series architectures. It should be possible to initialize any combination and configuration of memory, which includes 1 thru 8 NMB's. If this function fails any configuration, even intermittently, a failure should be suspected.

The most common cause of mminit failures involve the send portion (XS0 and XS1) of the crossbar. By use of the utility nmb_errs, it should be quite obvious whether the failure is address, or data oriented.

It might be helpful to understand that mminit acts very much like a simple memory diagnostic. This logic is further tested by means of subtests 380 and 385 of mem4000.

Failures of mminit indicating odd bank 15 of the last NMB installed are generally evidence of the need for a sysreset -l 2. The mminit utility will frequently fail in this manner if initall, or a sysreset -l 2 has not been accomplished. A standard sysreset will not usually be sufficient.

Al,

3.23.5 C3800 cu_ndat0_harderror Type Harderrors

Hard Errors of the type "cu_ndat0_harderror", or "cu_ndat1_harderr" are, quite often, an indication of a failure in some other area of the system and not necessarily with the NCU. These errors can be very misleading and not easily recognized.

Typically these failures do not occur as HARDERROR # 0 and are usually accompanied by memory input staging errors, or memory control errors. It is also likely that the memory failures can complain of data from a specific head. When this occurs, if the head is other than 0 than the failure will quite likely be a connectivity failure associated with that SP. If, on the other hand, the data originated from SP0 then it will not be as clear. This is because SP0 is designated in certain undefined conditions.

The utility 'xbar_err' can be very helpful in isolation of these failures. This utility will display all receiving boards that have encountered the data and where it's believed that the data originated. If memory input staging data errors are indicated in the display then the confidence will be quite high that the source is a connectivity failure with that SP, or a XS1 failure.

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If the problem is XS1 related then the problem will be movable by rotating the XS1 from one side (even, odd) to the other.

Only after XBar and connectivity problems have been ruled out, should the NCU be suspected.

The reason that these (continued)failures can be so difficult is because the NDAT gate arrays do not hold the correct error state and therefore will list multiple possibilities for failure location. A sample display appears below:

```
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE        PORT/SIDE      EXTRACTOR
-----------     ----------        ---------      ---------
    2            CU_TYPE            N/A          cu_ndat1_harderr
===================================================================
   NCU harderror detected
   ndat[1].ndat_harderr = 1
   ---------------------------------------------------
   Due to an NDAT design error, the NDAT does not hold it's error state
   correctly. The hard error has been detected and can be one of
   the following conditions:
   1) Parity error from the XBAR on the signals
      XSE_CU.WR_DAT<31..0>/XSE_CU.WR_PAR<3..0>
   2) Parity error from the NADR on the signals
      L1_WR_ODAT<7..0>/L1_WR_OPAR<3>
   3) Parity error from even comm register rams on signals
      CMR_RD_EDAT<31..0>/CMR_RD_EPAR<3..0>
```

In the case, above, only the XSE_CU.WR_DAT occurs external to the board. So, it should only be necessary to check these nets between the source and XBAR and the XBAR and NCU. But generally, if the connectivity problem rests on the NCU, or slot, then memory boards will not be involved.

The error analysis rules, sent in previous tech bulletins, can be very helpful in isolating this failure. As indicated, cpu test 4332 can help in further isolation of the failure.

If everything attempted appear ambiguous, or no change is seen then the failure, most likely, rests with the NCU.

Al,

3.23.6 Remove a Disabled NMB Before Booting a C3800

It is necessary to physically remove a disabled NMB before trying to boot the C3800. It is not sufficient to simply remove power from a defective memory board and otherwise leave the board installed.

If the NMB is left inserted in the slot, memory failures will be encountered when trying to boot to multiuser. It is also possible to encounter failures with diagnostics.

This does not apply to Sp's and Vp's. Simply removing power when disabling a head is sufficient to remove the failed head from the system.

Al,

3.23.7 C3800 Known Problems Progress

In an effort to answer the most frequently asked question related to progress on fixing the known problems with C3800's, this information is being made available. Please, bear in mind that these boards cannot be ordered based on these upgrades. This is for information purposes only. Below is a list of NSP revision levels and the problem intended to address.

C.1
Another attempt to fix nmul failures, this time tieing clk* to vref and moving clk out by ~400ps. Failing symptom is byte 4 ymux parity error on nmul, suspected to be a setup time problem on the nmul. Added to other function units as well. Also removes X.5 (function unit vref adjustment ecn).

D.0
Removes rev B completely. Installs three 0.01uF capacitors on pins (7 (Vref), 11 (Vcc), and 26 (Vcca)) to the lid (vtt) of the purge rams to reduce noise. Was wire revF xecn X.11.

Deletes clock delay wires of rev C and replaces them with 11 inch wires. Delays clocks to the function units an additional 1ns. Was wire revF xecn X.10.

Ecn to keep the branch history and referenced PRAMS from being able to cause hard errors, since they are non-destructive if wrong. Was wire revF xecn X.12.

Disable OLE on the dcache and ptecache prams by pulling it high. This helps the problem we were seeing where ring data does not match ram data on a pram failure, at first thought to be an access time problem. Was wire revF xecn X.7.

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Purge rams addressed in this release:
BR_HIST_L BR_HIST_U BR_HIST_XL BR_HIST_XU PRD_REF0 PRD_REF1

E.0
Turns off parity checking on purge RAM modify bits.

F.0
Hardware support for project to coredump processes that pull hard errors instead of crashing the complex. Need to guarantee that we don't hang the ncu because of pending traps; that we don't change the cir, tid, ring, idle status, and we keep interrupt state; and lastly we can't make requests to memory.

G.0
Disable parity checking on purge RAM lookahead valid bits.

H.0
Fixes assy revF problem where is used a register (spare8) that is held by some stram wr_par_err's. We now use register (stop_cntr) and the old stop_cntr is now (spare0).

Al,

3.23.8 C3800 SST V2.2.3

A new release of SST exists, version 2.2.3, which is intended to extend coverage to the rev H NSP. For all existing systems, the current v2.2.2 will continue to provide adequate coverage. All new systems will ship with rev H NSP's and version 2.2.3 of SST.

It should be remembered that the system has to be in a scannable state to execute successfully. This can be verified by executing a sysreset before execution of sst.

It is recommended, that the set limits off option be used, when executing sst on a C3800. This option is used so that sst will not abort on encountering the first error. As failures are quite often encountered, particularly with the NIA, this will save valuable time in the packing and execution phase.

Al,

3.23.9 Powering Down the NCU or XBAR

If, for any reason, it is necessary to power the NCU and/or XBAR down, then it will be necessary to perform a sys_shutdown and diaginit before attempting to boot the system. Just relinking the NCU and crossbar with diaginit will not be sufficient to restore scannability of the entire system. In many cases it will even be impossible to mminit if the entire system is not reinitialized before continuing.

Al,

3.24.1 Defective C3800 Keyswitches

It has been discovered that some defective keyswitches exist on installed C3800's. The keyswitches are defective in different positions and can cause individual bays to power down when moved from one position to another. This in turn will cause the system to crash.

If this problem is encountered, it is recommended that the keyswitch be replaced. The part number is 500-000416-202.

Dan Brenner

3.24.2 C3800 I/O Bulkhead Connectors

In order to save money, we will no longer ship an IDC bulkhead in each unused I/O slot, on C3800's.

From this point forward only one unused IDC bulkhead will be shipped with new systems. This extra one can be used for troubleshooting purposes and make upgrades easier. For maximum benefit, the spare will always be installed on the unused Pbus, if one exists. If not in use, this will always be on Pbus 2, or 3. This will make it far easier to move a CCU and power to this side and verify functionality.

In addition, the unused augat, XIOP slot, in bay 4 will be removed as a cost savings measure. The combined savings for these two measures will be $1480 per system. For systems already installed, this augat can be used as a spare if deemed necessary.

These cost savings, when applied to only the existing backlog, amount to nearly $50,000.

These measures should have little impact on the field and has significant benefits for CONVEX.

Al,

3.24.3 Replacement for C3800 fujipoly

Within the next 30 days CONVEX should be shipping, with new systems, a replacement for the current fujipoly used on 3800's.

This replacement is known as ecpi (elastomer conductive polymer interconnect). It is manufactured by AT&T and has vastly superior handling characteristics when compared to the fujipoly.

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The primary difference is that the ecpi utilizes stacks of 3 mil ball bearings opposed to the 20 mil wires used in fujipoly. Most cleaning problems associated with the fujipoly involve loose wires from the material itself. With the ball bearings this eliminates that problem, as the bearings are too small to short between pads.

In addition the new material does not attract dirt and in most cases requires no special cleaners prior to installation. Generally, dusting the material off is sufficient to remove most contaminants.

The ecpi has the additional quality of being slightly sticky on one side which seems to hold it in place during installation.

If all goes well, the ecpi should be installed on new systems built after 15 July.

The fujipoly already installed will not be replaced, except as wear and failure dictates.

Al,

3.24.4 New IDC Diagnostic - idc4010

The diagnostic idc4000 has now been replaced with a new and improved version called idc4010. This new diagnostic has greatly enhanced functionality and test capabilities. It will be released with v1.1 of the I/O diagnostics for C3200 and 3400's.

This diagnostic has test suites for the ITC, has loopback capabilities with modified jumpers and interactive debugger capabilities.

The part number for the idc4010 diagnostic manual is 760-007030-000 and should be read for an indepth understanding of the diagnostic and its capabilities.

Al,

3.24.5 Scan Based Test Failures With REV H NSP's

Now that the rev H NSP's are arriving in the field as replacements, it should be understood that certain failures can be obtained with scan based tests such as spu4000 and SST.

The diagnostic spu4000 will fail subtest 710 and subtest 810 if run with all available boards installed. If spu4000 is executed on only the rev H NSP and necessary other components (i.e. ncu and xbar) then it will pass.

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Version 2.0 of diagnostics and 2.2.3 of SST will rectify the problem.

Al,

3.24.6 FMI-0092 for C3400-ES B3 Faults

FMI-0092 is available immediately for installation in C3400-ES systems that are experiencing intermittent B3 errors.

The FMI replaces the lower front VME chassis card cage bar with a new low profile part. Airflow through the chassis in the area of the VBCU airflow sensors is increased significantly.

The FMI should be installed in all C3400-ES currently installed. All systems shipping this quarter have been upgraded by manufacturing.

* Dave Muir *

3.25.1 Installing C3800 SpuOS 2.0

The install procedures in appendix A of the Convex SpuOS v2.0 release notes needs some corrections.

Appendix A step 4 should read:

Step 4: tar cvf /dev/rst0 /ioconfig /etc/hosts /etc/passwd /mnt (and any other files you have modified)

Appendix A step 7 thru 9 should read:

Step 7: su (to become root)
Step 8: cd /
Step 9: tar xpf /dev/rst0

Dan Brenner

3.25.2 Loading tli4480

It is recommended that the diagnostic /diag/test/tli4480.t be saved, prior to loading tli software on the JP. The TLI software installation will copy a new version of tli4480.t to the SPU and this version will not execute.

After loading this software on a C3800, it is then possible to copy your saved version over that downloaded during the tli software installation.

Al,

3.25.3 C3800 xsysconfig

Please remember that it is possible to change C3800 hardware configurations by means of the xsysconfig feature. This will allow both NMB's and heads to be removed and reinstalled from boot configurations without having to power down the head and memory boards. This will save wear and tear on the components themselves.

When using xsysconfig to modify configurations, it is possible to encounter memory timing errors and memory faults at boot. Ignore these and continue with the boot. These failures are not fatal and should cause no problems after the system is booted.
Al,

3.25.4 Monitoring C3800 Powered Down Bay Detection

As a suggestion, it might be beneficial, for troubleshooting purposes, to cut 2 to 3 inch strips of mag tape and tape to the top of C3 bays. In this way, any powered down bays can be spotted very quickly. With the noise, usually associated with computer rooms it is near impossible to tell if a single bay has powered off. This can result in serious delays in identifying the cause of a crash or failed boot.

Of course this doesn't help in the case of a remote session, but individuals are generally more cautious and observant when dialed in.

Al,

3.25.5 Running spu400 with Multiple Rev H NSP's

It may not be possible to run spu4000 successfully when multiple rev H NSP's are installed in a configuration with other lower rev NSP's and running v1.1.2 diagnostics.

The recommended procedure for executing spu4000 when rev H NSP's are installed, is to configure all boards except NVP's. Leave the NVP's out of the configuration. After the test is run, then disable NSP's and memory and enable the NVP's and execute spu4000 subtest 810. This will afford the best chance of success.

It is still possible to encounter failures with subtest 710, 713 and 810. Although, with a single rev H NSP, this is unusual.

In the case of multiple rev H NSP's, it may require powering the rev H boards down and executing the tests and then powering the other heads down while executing on the rev H boards.

If problems are encountered executing spu4000, it will be necessary to completely exit the diagnostic before attempting to execute again.

The important thing to remember is that if failures are encountered with spu4000, it may be due to rev H NSP's in the system.

Because of these failures, an attempt will be made to expedite v2.0 of the diagnostics and 2.0 of spu unix.

Al,

3.25.6 FDDI Firmware

It is important to understand that the firmware download to the FDDI controller is accomplished by means of the /mnt/os/drvfsd.conf file. This file is located on the SPU.

The download of the firmware will fail, at probe and attach, if this file does not exist. It should be created when loading the FDDI driver. The error will indicate a failure to access this file. It is also possible to comment the download entry out, in this file and force a probe and attach with the Eprom code. However, the controller will not function properly without this download succeeding.

It is intended that all firmware downloads will be directed with this file in the future, but for now FDDI is the only device that uses it.

Al,

3.25.7 Two Types of DAT Drive

It is important to understand that logistics currently stocks two different versions of the DAT drive.

The first being a differential drive that is used with the standard SCSI Host Adapter. The part number for this is 207-000017-200.

The second drive is a single ended device used with the C3800 SPU, only. The part number for this drive is 207-000018-200.

Al,

3.25.8 ConvexOs 10.0 and VIOP Page Allocation

It has been discovered that the VIOP device associated page allocation numbers with 10.0 appear to be less than accurate. Currently, it is not known how extensive the problem is, but until more is understood, caution should be used when adding devices to existing configurations.

As a temporary work around, it is possible to use different tunables associated with the ethernet controller. It is suggested that this be attempted if a configuration does not have sufficient memory for a configuration that should work, with the existing documentation.

The solution to this problem is being pursued and we will notify you of the correct information.

Al,

3.25.9 Removing Boards On C3800

It is recommended that when removing individual boards from a head on a C3800, that the accompanying board be backed out of the backplane. For instance, if removing a NSP to return to Dallas, then back the NVP out as well.

The reason for this is that some interaction with the remaining board, even though powered off, has been associated with intermittent spu4000 failures and in isolated instances, even system crashes.

Al,

3.26.1 C3800 wredc Parity Errors at Upper Clock

It has been discovered that memory wredc parity errors will occur when running a C3800 at upper clock. The failure will always indicate BANK 0o and can occur on any NMB.

An example of the error can be seen below. As indicated this error should be the only hard error reported at the time of the failure.

The cause of this problem is being investigated, but until it is solved, please bear this in mind. The clock frequency at the time of the crash can be confirmed from the output of the hard logger, directly after the cop is completed.

Hard error Summary

```
------------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE    EXTRACTOR
-----------     ----------          ---------    ---------
    0             MB_TYPE               0         mb_odd_bank_wredc_par_err
========================================================================
 ODD side 'bank_wredc_perr': PARITY error detected in MB6
------------------------------------------------------------------------
 WREDC PARITY error detected by BCGA 0 in bank 0 ( => BANK_0o)
 during a READ.
   -----    --------------------------------
      1       mbs6:bc[0].sys.bctl0_merr_pe
      1       mbs6:nmc0o_rerr
      1       mbs6:nmc0o_rla_ecc_check1
  10480000        mbs6:nmc0o_data
         f        mbs6:nmc0o_ecc (parity)
         1        mbs6:bc[0].bcga_log.bctl0_cycle
     e7e6e0       mbs6:bc0_bank0_log_addr (phys_addr is 73f3700)
------------------------------------------------------------------------
```

Al,

3.26.2 PETS Version 3.0

A new version of PETS, v3.0, has been released. This version is executable on all C based CONVEX systems.

With this release, test 14 and 15 will now indicate that they will not execute. In past releases these test would indicate that they were run once and not repeat. These tests will not execute on disk frag sizes above 1K.

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On C3800 systems it will be necessary to comment test.046 out of the scripts and move the module, in the Processes directory, to test046.sav. This is necessary because this test module is defective on the released version. This test was designed to test STRAM's on 3400 and 3800 systems and is not utilized on C1, or C2 systems.

If test.046 is not removed from the scripts a core dump, indicating nonexistent file, will occur.

Al,

3.27.1 Trouble Shooting C3800 Power Problems

The process of troubleshooting a power problem can be an easy one if the proper procedures are followed and the tools are used to the fullest advantage. This is intended to be a guide to aid in the isolation of the source of power failures.

Below is the output from pwr_util, using the "n" option for display of the status of an individual power pallet. As can be seen below, ppc #2 has been selected, which as explained in the "C3800 Troubleshooting Hints" Chapter 6 Article 4, is NSP0. It is recommend that this article be read at this time to get the total benefit of this power discussion.

The utility pwr_util can be complemented with powermon, but this status display will contain everything that is necessary.

```
spu> pwr_util

a) Bpc chk interlock  b) Reset uart     c) Bpc reset      d) Init bpc
e) Offline bpc        f) F/W revision   g) F/W Download   h) Bay Config chk
i) Cop Read           j) Cop Write      k) Bay Power chk  l) Power On
m) Power Down         n) Send Status    o) Set voltage    p) Set temp
r) Busses off         t) Transparent
q) Quit               ?) Print Menu

Enter command: n
Select uart channel [0-4]: 0
Select ppc id [0-8] where 8 indicates bay controller only: 2

+++> <Tue Jun 30 08:02:55 1992> pwr_util:../pwr_util.c:230
SW Info (DiagIN238): Power Pallet Controller status message

PPC Status
fill  fw    pp  open err err  plt bd bd bd bd bd bd bd bd slot warm hot bus
byte state fail ilck grp code id  0  1  2  3  4  5  6  7   id  flag flg trim
00    02    00   00   f1   1f  02  02 00 00 00 00 00 00 00  07  00   00   00

bus_on brick brick brick brick tmp0 tmp1 tmp2 tmp3 tmp4 tmp5 tmp6 tmp7 A/D
error  exist type  fuses input snsr snsr snsr snsr snsr snsr snsr snsr over
00     3fff  3bdb  0000  0000  57   58   58   56   54   5b   5e   5a   00

hous A/D0 A/D1 A/D2 A/D3 A/D4 A/D5 A/D6 A/D7
volt cnvt cnvt cnvt cnvt cnvt cnvt cnvt cnvt
00   f7fe 0813 ffff f7ad fcb8 fce2 fffe f8ca
****
```

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Below is a list of definitions for entries in the example above:

1) brick exist - A "1" is set for every brick installed on the pallet. A different bit is used to represent each brick installed. The below list is used for all brick and fuse status. Where S10 is slave supply 10 and M1 is master supply 1.

S10=0001 S9=0002 S8=0004 S7=0008 S6=0010 S5=0020 S4=0040 S3=0080

S2=0100 S1=0200 M4=0400 M3=0800 M2=1000 M1=2000

example: 3fff indicates that all supplies are installed.

2) brick input - Is the opposite of brick exists, as a "1" indicates that the individual supply is turned off. This is a great aid in determining which power busses are defective.

3) brick fuses - A "1" indicates which fuses are open. In addition to the list of supplies above, this entry has two additional bits.

FUSED300V=4000 INPUT300V=8000

4) brick type - This entry will indicate the type of bricks installed, where a "1" indicates a 2V brick and a "0" indicates a 5V brick.

The A/Dx fields are a 2's complement hex equivalent representation of a DC voltage level. To convert to a DC voltage the 2's complement hex value converted to decimal and multiplied by 5/2048. It is important to understand that values of the 0xxx is positive and fxxx is negative.

Example: A/D1 = 0813 converts to 2067 decimal * 5/2048 =5VDC
A/D0 = f7fe converts to 0802 hex and 2050 decimal * 5/2048=-5VDC

Those values that are a 0000 would generally indicate a shorted input. The master supply would be suspect here. A value of ffff would mean that this bus does not exist on this board.

The table below indicates the bus covered by each A/D circuit on a board by board basis.

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BOARD	A/D0	A/D1	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7
NMB	PPCM5V	PPCVCC	GND	GND	VTTGA	VTT	VCC	VEE
NSP	PPCM5V	PPCVCC	GND	VEE10K	VTTGA	VTT	GND	VEE
NVP	PPCM5V	PPCVCC	GND	GND	VTTGA	VTT	0	VEE
NIA	PPCM5V	PPCVCC	GND	VEE10K	VTTGA	VTT	VCC	VEE
NCU	PPCM5V	PPCVCC	GND	VEE10K	VTTGA	VTT	VCC	VEE
XBAR	PPCM5V	PPCVCC	VEE	VEE	VTTGA	VTTGA	VTT	VTT
CCU	PPCM5V	PPCVCC	GND	GND	M5V	VTT	VCC	VEE

```
Where: M5V = -5VDC
       VCC = 5VDC
       VTT = -2VDC
       VEE = -4.5VDC
       GND = 0VDC
    VEE10K= -5.2VDC (STRAM's)
    VTTGA = -2VDC
```

The temperature sensors located on the boards (tmp0-7) indicate the fahrenheit temperature in 10mv increments. The conversion is as follows:

adc counts * (2.5/.01*255)
2.5/.01*255 = .98
adc count *.98
convert hex value of adc count to decimal and multiply by .98.

Example: tmp0=57 0x57 converts to 87 dec.
87*.98 = 85.26 degrees F

The other fields can be identified by use of the C38XX Power System Firmware Description.

With this document and the Firmware Description, it should be relatively easy to identify and correct Power Pallet related failures.

Al,

3.27.2 Installing HiPPI in a C3800

It should be understood that to install HiPPI in a C3800 an assembly rev B CCU Power Pallet is required.

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To verify that the correct power pallet is installed in the system, it is only necessary to remove the cover and examine the part number tag affixed to the front of the power pallet. If it is HiPPI compatible the label will indicate (HIPPI). If the label does not indicate this then the incorrect CCU Power Pallet is installed for HiPPI support.

Al,

3.27.3 C3800 STRAM Failures

The STRAM failures have become the predominant problem with the C3800. The reason that they have become the prevailing failure is due to the other problems being brought under control.

The STRAM's are generally used in the caches and control stores on the NSP. They have their own power bus, 10KVEE (-5.2VDC). STRAM's are also used on the NCU in the comm registers and on the NIA in the data buffers.

Below is a list of STRAM associated hard errors. Due to the nature of the failure, a single occurrence of a STRAM hard error is usually sufficient to justify replacing the NSP.

STRAM WRITE ERRORS (errors detected by strams - input data)

```
sp_dcd0_wr_par_err -dcache data
sp_dcd1_wr_par_err
sp_dct0_wr_par_err -dcache tag
sp_dct1_wr_par_err
sp_dcu0_wr_par_err -dcache update
sp_dcu1_wr_par_err
sp_icd_wr_par_err -icache data
sp_ict_wr_par_err -icache tag
sp_lat_wr_par_err -icache lookaside tag
sp_pted0_wr_par_err -pte cache data
sp_pted1_wr_par_err
sp_ptet0_wr_par_err -pte cache tag
sp_ptet1_wr_par_err
sp_srd_wr_par_err -sram data
```

STRAM READ ERRORS (errors detected by device receiving stram data - output data)

```
sp_nrfa.extdata_par_err -sram data
sp_npa0.ctag_par_err -dcache tag
sp_npa1.ctag_par_err
```

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```
sp_ndp0.cupd_par_err -dcache update
sp_ndp1.cupd_par_err
sp_ndp.yuvc_crd_err -dcache data
sp_nrfa0.nrfa_wcs_par_err -wcs
sp_nrfa1.nrfa_wcs_par_err
sp_nrfa2.nrfa_wcs_par_err
sp_nrfa3.nrfa_wcs_par_err
sp_npsw.npsw_wcs_par_err
sp_nus.nus_wcs_par_err
sp_nag0.uirl_par_err
sp_nag1.uirl_par_err
sp_ndc.uirl_par_err
sp_npa0.pdata_par_err -pte cache data
sp_npa1.pdata_par_err
sp_npa0.ptag_par_err -pte cache tag
sp_npa1.ptag_par_err
sp_npar.inst_tag_par_err -icache tag
sp_npar.look_tag_par_err -icache lookaside tag
sp_npar.que_par_err -icache data
```

Al,

3.27.4 APR and ConvexOs 10.2

As most of you have noticed, in the C3800 status report, there is mention of APR and 10.2 OS.

The APR utility is to allow the removal of a single head from a C3800 complex after failing. This will be accomplished automatically and is intended to have minimal impact on the system and customer.

The idea is that when a head fails for any reason, the process executing on that head, at the time, will be terminated and the head will automatically be taken off line. This will leave the remaining heads active. The failed head will then be able to be fixed, or replaced as necessary and be returned to the complex at a later time. Initially, it will not be necessary to return the processor to the complex without taking the system down, but this should be available at a later date.

The components required to support this function will be 10.2 OS, rev H of the NSP, a wire add to each processor backplane and 3.0 of the diags.

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A reboot of the head will be determined by successful completion of SST. Because the possibility exists of not having correct patterns loaded, an option will be left to re enable the head manually using cpuconf.

When each site will have this functionality will depend on when all heads have been upgraded to rev H of the NSP. As mentioned previously, the rev H upgrade will commence towards the end of July. The OS will not be available before August.

Please do not attempt to escalate your individual sites on the list, as it will be scheduled as soon as possible. It is expected that the upgrade will take 4 to 6 months to complete.

All systems shipped after 15 June have the required hardware installed, but will not be able to use the function until the OS and diagnostic support is released.

More will be explained on this matter as the time approaches.

Al,

3.27.5 C3800 Memory Boards Dropping Off Line

During periods of troubleshooting, or system reconfiguration, it is possible for memory boards to actually drop off line. This means that the NMB remains powered up and for all practical purposes, is physically in the configuration, but for purposes of use it is not available.

The symptoms will be that the NMB shows up with no problems after the diaginit is executed, but mminit does not run on the NMB, or after booting the system, the NMB is unavailable.

This problem, though somewhat frustrating, is easily solved.

By using the sys_config window it is quite quickly seen that there are two sections. The top of the display indicates components physically installed in the system and the bottom half displays components that are not available to OS. It will generally be found that the offending NMB's are not available for OS. To solve the problem, it is only necessary to click on these entries with the mouse and after an initall, this will restore all available components to the configuration.

Al,

3.27.6 Updated C3800 Shipping Container

There is now an updated version of the C3800 shipping container in use.

The improvements are as follow:

1) Improved foam positioning
2) Foam modified
3) Foam thickness same on all sides to prevent board damage
4) Handles on both ends of box
5) Better labels

The original containers will remain in service, as they cost $450 apiece, so don't be surprised.

In addition a set of metal tubes will be included in the boxes. These tubes are to be slid over the rails of the board before it's placed in the box. These tubes are to provide rail reinforcement during shipment to prevent damage that has been seen on returned boards.

Al,

3.27.7 First Shipments of C3400-EX

The first C3400-EX (Extended 8 head chassis) systems shipped near the end of the second quarter.

There are some know diagnostic failures is you run individual diagnostic tests.

PETS	Appears to stop running. When this happens the scheduler and interrupt handler are taking almost all available cpu cycles. This problem is still being investigated.
cpu4241	System hang while running cpu4241 parallel mode. This is only a problem with 4236 JCPUs when running more than 2 heads.
cpu4041	For 410-001236-200 JCPU boards increase the time delay to 10 in all cases.
cpu4331	This test will fail when running this test in ring 4 force fault mode.
cpu4331	The following tests will fail. Subtest 26, 27, and 30.
cpu4332	Subtest 259 will fail when run in ring 4 force faults mode.

.....continued on next page.....

cpu4332 Subtest 246 will fail.
cpu4333 The following subtests will fail. Subtest 473, 478, 1021, 1026, 1035(8 head) and 1036.

Diagnostic Release V1.2
New utilities have been added:

mi_func	This utility replaces an iscn script that has the following usage: mi_func -c <#> -q <re[questq]|ro[q]|xf[erq]|ca[che]|co[mmq]>
mmap_mcm3	This utility performs the mmap functionality but is used with mcm3 memory pairs.
enable_rt_cpus	This utility will set the mode for a head to be real-time. This is only useful when used with the Real-Time Operating System.
disable_rt_cpus	This utility will deselect the mode for a head to not be real-time. This is only useful when used with the Real-Time Operating System.

Enhancements:

The loader and initialization portions of the cpu tests has been changed to decrease the amount of time for loading and initializing the cpu tests. This speed up is noticed in multi-headed loading.

Utilities Fixed:

dcache	Modified "dcache" to display parity errors only for the specified range of addresses.
pte_cache	Modified "pte_cache" to display parity errors only for the specified range of addresses. Fixed a bug that prevented all of the pte_cache from being displayed.
ipte_cache	Modified "ipte_cache" to display parity errors only for the specified range of addresses.
map	Modified "map" to expect the cir and tid numbers to entered as hexadecimal numbers. Added an extra option (-f) to display the addresses of the ptes.
mm	Modified "mm" to display the new C3 instructions and to use the new cpu test loader format.

.....continued on next page.....

cs	Modified "cs" to display a message when no cpus are configured, and added a function to the utility to store the microcode revision information in a file UCODE_REV in the /mnt/usr/ucode directory.
commreg	Modified "commreg" to not check disabled heads and changed the crashdump method to only dump the commregs from the lowest numbered and configured cpu in the complex.
hard_logger	Modified "hard_logger" to display the serial number of the head that took the error. Also added more intelligence to the "hard_logger" in regards to MCM reported hard errors. 1) When a MCM hard error occurs now the "hard_logger" will double check to ensure that the "err_type_log" scan field on the MCM3 is correctly indicating the hard error that really occurred. Discovered that this scan field is not always correct. 2) For write data parity errors the MCMs will now report which port that bad data was on.

Test Programs:

Modified cpu4030, cpu4041, cpu4241, cpu4331, cpu4332, and cpu4333 to also output the hard_-logger information to a file when the test information is being sent to a file.

Utilities Bugs:

mm	when a hard error is present "mm" will not work properly without doing a "sysreset" first.

Thanks to many people in engineering and manufacturing for this information.

* Dave Muir *

3.27.8 Disk Errors When Dumping a "C" Partition

There have been several reports recently of the following disk errors during a "dump" of a C partition

.....continued on next page.....

[CCU01@01:31:19]dd3: RD :Bytes/sec spec error (0x51) (ERR:0x51)
[chs=1623/14/82]

This error has only been seen on Saber5 drives on the SMD controller, but it may be possible to have this error on other SMD disk drives.

Until a resolution to the problem is found, a temporary work-around is to use "xdump" in place of "dump"

* Dave Muir *

3.28.1 Corrupted C2 Database

It is quite common during the course of a reconfiguration, or troubleshooting effort to get the data base of a C2 (3200) in an unusable state. The symptoms of this would include: a missing head, failure of initall, mminit, or .diaginit. It will generally appear as a memory configuration that is much larger than physically installed, or failure to recognize a newly installed head.

To clear this type of problem, the following reset sequence is recommended:

1) mminit -f (In the case of mminit failures, this will force an init of physical memory, ignoring the pcm contained in the boot_db)

2) cp /mnt/os/boot_db to a file

3) rm boot_db

4) mkdiag_db -a (This will force the configuration parameters to be remade into the existing configuration.)
   mkdiag_db -p (This will print the current configuration parameters.)

5) scn_util -i (Initializes clocks to memory and I/O.)

6) scn_util -b > /mnt/os/boot_db
   (To download configuration to boot_db.)

7) initall

This sequence should enable recovery from most data base, or configuration related failures.

Al,

3.28.2 Changing mm_sniff Sniff Rate

It is possible to increase, or decrease the mm_sniff rate on CONVEX systems. The default sniff rate is 32 MB/day. When increasing the sniff rate, it should be understood that any increase will impact system performance to some extent. To increase the sniff rate proceed as follows:

.....continued on next page.....

Edit the file /mnt/os/boot and add a "-r xx" entry to the errintd startup in this file. Where xx is the number of MB to be sniffed in a 24 hour period.

The change to 64MB/day would appear as follows:

```
prtlog
#
# Don't want to start errintd from prtlog on C38's, so start
# it here by hand if /diag/bin/errintd exists (ie, if on C38).
#
if [ -f /diag/bin/errintd ] ; then
/diag/bin/errintd -h -s -r 64 &
fi
$bootcmd || exit
```

This change can be used to accelerate the mm_sniff process when a memory problem is suspected, or the physical memory size is sufficiently large to preclude mm_sniff from ever completing.

Al,

3.28.3 EPROM Damage When Powering Down A NIA Board

Manufacturing has reported that on some occasions after powering down the NIA board, the eprom gets blown on the ccus (primarily the IDCs) in the right ccu backplane when powering the NIA back up (The left ccu backplane is powered by the same bps as the NIA but the right backplane is powered by a separate bps.)

Based on these observations and until further analysis can be performed, it is recommended that the NIA not be powered down without also powering down the right ccupp for those C3800 systems having ccu boards installed in the right ccu backplane.

Jerry

3.28.4 C3400 Diagnostic Bug.

spu4000 will fail st4118 if it is run immediately after doing an initall.

If you are going to run spu4000, the following sequence is necessary to insure that the test will run correctly. After the initall, but before starting dshell, do a 'sysreset' followed by a sysreset -l2.

After running spu4000, it is necessary to do a '.diaginit -f', or 'load_clk' and 'initall' before attempting to boot the system.

This bug will be fixed in a future release of diags.

* Dave Muir *

3.29.1 No Information for the Bulletin This Week

3.30.1 SST Version 3.0

The newest release of SST (version 3.0) will soon be available in the field.

The primary enhancements in this release are support of APR and decrease of sensitivity to board revision changes.

In support of this there are 2 new entries visible with the cop:

```
Machine  Device     Part       Serial   Ring    Wire   Assm   DC   AC
  Slot    Type     Number     Number   Rev     Rev    Rev    Rev  Rev

  sp0       sp  416-006247  1036575    1       F      D      9    0
```

As seen in the example above, the DC rev alone will now be used to determine the static pattern tests to execute on each board. In the past, it has been far more complex in using all other revision information to make the choice. This will allow hardware changes that don't require pattern changes to be made without affecting SST. This DC rev will be included in the cop info.

The new release will still be downward compatible with previously released boards and will indicate the old method to be used by a DC Rev value of 0. All board releases from now on will require a valid DC entry in the cop chip. A 0 value will not be valid for new releases.

The AC Rev will be used to support CAST based in house testing and will not be utilized in the field.

The second major enhancement will allow testing to be performed online. This is a major component of the APR. This will allow SST to be executed on a board, simply by removing it from the OS. All other heads and memories will remain operational while this is done. A head can be removed from the system by use of the command:

cpualloc the -d option will be used to deallocate the head
the -e option will be used to enable the head

NOTE It is assumed that the head is in a quiescent state when it is disabled.

The following errors are supported with this release:

.....continued on next page.....

1 Illegal argument passed to cpualloc
2 Unable to reserve specified CPU
3 Specified SPU is unavailable
4 Init of CPU failed
5 sc_init failed
6 CPU is not hung, cannot deconfigure
7 Cannot configure a running CPU
8 Cannot deconfigure a non-running CPU
9 Invalid data for head 0 in configuration database.

It should be noted that the xbar, NCU and NIA must be present for operational systems. It will not be possible to remove these boards from the complex, for obvious reasons.

Because of changes to the CDB, it is possible to execute SST on components unassigned to OS simply by entering "run sst" in /sst directory. All files will be packed as necessary and executed on the appropriate boards. Because of modifications, sst cannot crash a system. It is possible to remove a component from OS assignments by the use of xsysconfig.

Booting the system will make all currently assigned components untestable by sst. It will not be possible to remove the component from the complex on line, unless it has failed. If it is desired to execute sst on a component of the complex, that has not failed, it will be necessary to remove it from the complex with xsysconfig prior to booting.

It will, however, be possible the re-enable a downed head by the use of cpualloc and cpuconf.

It is intended that APR will automatically deallocate a failed head and execute sst and if passing will return the head to the complex. The decision to execute SST and the number of failures tolerated are software selectable.

Previous SST functionality is supported and can be reviewed in past tech bulletins and the SST Users Guide. Specifically article 21 of chapter 2 of the "C3800 Troubleshooting Hints" will be helpful in this review.

***** NOTES *****

When executing multi board data tests involving the crossbar, failures will occur if hardware in the system has been powered down. This will not occur on single board tests.

When executing multi board tests at the SPU, it is necessary to perform a sysreset before initiating SST testing.

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When encountering multiple, between board, failures, it is best to confirm basic continuity of these circuits with spu4000. This is because SST assumes the basic continuity between boards is present.

The following parameter settings should be understood by the user. These are explained further in the "Handbook" and the "SST Users Guide".

1) test limit total
2) test limit stop
3) test limit eliminate
4) test limit board
5) disp failure pins

Al,

3.30.2 C3800 Diagnostics Version 3.0.0.6

Now that the revision 3.0.0.6 Diagnostics is being released, it's time to explain some of the differences and enhancements produced for this release.

This revision will be required for support of APR and the version 3.0 SST which will be explained in other articles.

Enhancements:

1) add_parts - A new utility that interrogates the /diag/db/part_numbers file and makes necessary additions to the Configuration Data Base.

2) cop/copmod - Modification used to support changes in 3.0 of SST. The new cop and copmod will now list DC and AC rev levels for all boards. This info will be used to determine the correct SST patterns to run on boards, rather than the old method utilizing ring asm and wire rev's to determine board pattern type.

3) ddb - Added -i option that allows ddb to use current page_map info to allow ddb to be used on currently loaded CPU jobs.
Added breakpoint capability within CPU code.
Supports trace traps.

4) Diaginit - Checks installed NSP's for support of APR. Will update the dynamic_cpu_harderrs_n entry in the CDB.

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5) Errintd - Changes required for APR.

a) Includes, only, non APR functional heads in hard error mask.

b) Added support to check for hard errors on heads that are APR functional.

c) Places APR related messages in the errlog.

d) Added support for XCL2 to clear soft errors after processing the error. This will allow additional soft error support on the XCL, but is not required for APR.

6) fw_rev_update - Updated to reflect new loaded firmware which is 3.16. The new bpc_firmware fixes a problem of processing non existent bays and timeout failures between ppcs and bpcs.
ppc firmware is now at 2.8 and fixes problem of report of 300v out of range continuously. Now reports once.

7) hard_logger - Adds -m option to process CPU's that do not have APR function enabled.

8) mminit - Modified to detect 1/4 populated NMC's
Added -t option which denotes timing info in CDB.
All changes to support NMB2.

9) CDB entries for APR support:

enable_cpu_harderrs
cpu_hard_err_sniff_period Discussed in APR Article
dynamic_cpu_harderrs_n
cpu_automatic_realloc_n

Other new entries:

mb_installed_dram_sizes_p_n (n=0-7) Specifies size of drams on NMC.
mb_installed_dram_rows_p_n (n=0-7) Specifies number of rows on dram on NMC.
head_0_mm Data captured from SP0 after a hard err is detected.
bank_intrlv_sel_n (n=0-4) Specifies interleave where 0=1 bank 1=2banks, 2=4 banks, 3=8 banks and 4=16 banks
cpu_running_os_n (n=0-7) Denotes cpu's running OS.
enable_1x_purges Enables a 1x purge of rams instead of 2x.

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10) ucode_rev_update - SR is now at 10.6 and US advances to 10.36. Others remain at 10.0. Changes support APR.

11) xsys_config - Added capability to disable cpu hard errors. A new submenu that allows users to specify bank interleaving.

12) mem4000 - Support NMB2

13) spu4000 - Updates subtest 810 to test CPU backplane hardware change required for APR.

Fixes:

1) bpcwachd - Modified error handling to match firmware.

2) copmod - Allows CCU's to be cop modified.

3) cpualloc - Fixed to allow heads to be dynamically added and removed from the system with OS running.

4) ddb - Fixed interaction problem with VM register.

5) diaginit - Modified to set osc_freq in CDB to 16.7ns after oscillator speeds have been determined.

6) errintd - Modified so errors processing memory soft errors do not cause termination of errintd.

7) hard_logger - Screen saver option stars after keystroke or mouse event rather than waiting for next boot.

8) swix_load - Corrects SWIP download failures.

9) mminit - Logs errors in event logger. Initializes new memory related entries in CDB. Will indicate actual size of NMB.

10) mem4000 - Fixes subtest 366 to allow different size NMB's to be tested.
Fixes subtest 500 to test all of memory.
Fixed error checking failures in subtest 366.

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11) xdiag/cpucti - Fully functional and support all CPU diagnostics.

Utilities fixed and/or modified in this release:

1) copmod
2) cpualloc
3) errintd
4) mminit
5) xsys_config
6) cop
7) cop contents

Al,

3.30.3 C3800 APR Utility

The new utility, APR (Automatic Processor Recovery), will soon go into field beta test at selected sites. With this in mind, the following explanation of operation and functionality is offered to prepare the field for its use:

APR prerequisites are as follow:

1) 10.2 OS
2) FMI 93 (backplane upgrade and copmod)
3) Rev H, or above NSP
4) rev 2.0 SPU Unix
5) rev 3.0.0.6 Diagnostics
6) rev 3.0 SST

The intent of APR is to allow a single C3800 processor to be automatically disabled on a hard error. Other heads in the complex will continue to function uninterrupted.

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Because of the data base modifications, it will be possible to run APR on systems where all heads are not at sufficient rev. In this case only heads at rev and with backplanes properly upgraded will be re-enabled on failure.

The user process running on that head will be terminated and a core file created. All other processes will be unaffected. If the user process is executing a system call on the failed head, then the process will be signaled and continue to execute normally. Again, only process executing in ring 4 are recoverable.

If the kernel is executing on the failed head then the system will panic. The panic will be:

ConvexOS:FATAL ERROR:(Sched 8825)irrecoverable hard error: context jump not set

The object of APR will be to deallocate the head, execute SST on the failed head and if it passes, return the head to operation. All options as to number of failures allowed and whether tests are run are fully selectable by the Convex Field personnel.

The heart of APR will be the cpu_monitor daemon, which will monitor the state of the processors on a regular basis. The default will be 60 second intervals. The cpu_monitor daemon will be started in the rc.local file.

The cpu_monitor daemon will be programmable from the file "/etc/cpu_monitor.config file. This file is displayed below:

```
AUTO_REENABLE = 0;   # 0 Indicates no auto re-enable
SST_ENABLE = 1;      # 1 indicates run SST before re-enable. If the head fails SST then the
                     head will not be re-enabled.
FAILURE_COUNT = 0;   # 0 indicates that unlimited errors will result in restart. Any other
                     value will indicate number of retires in the below time period.
FAILURE_COUNT_TIME_LIMIT = 24 # Indicates time limit for failure count.
```

Additions have also been made to the CDB to support APR:

```
enable_cpu_harderrs -          0 will allow APR functionality, 1 will enable normal error
                               processing.
cpu_hard_err_sniff_period -    Used bu cpu_monitor daemon to control monitor interval (In
                               seconds).
dynamic_cpu_harderrs_n -       Indicates if CPU and backplane for each head support APR.
```

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cpu_automatic_realloc_n - Specifies whether to automatically re-enable failed head.

The backplane modification will consist of a single net from the NVP to the NSP which will inform the NSP in case of a NVP hard error. The backplane must be cop modified to indicate the presence of this net before APR can function.

To determine if a head is APR capable it is, only, necessary to perform:

cdb_get dynamic_cpu_harderrs_n, where n is the CPU number

A value of "1" indicates that the head is hardware capable.

A new switch is available, in xsys_config, to allow the enabling and disabling of APR/CPU hard errors.

The utility cpuconf <-e, -d> can be used to disable a head from the OS complex. When the head is enabled, control store load and sysreset will be automatically performed on the individual head.

Execution of sst will be controlled by the file /diag/hw/cpualloc.test. This file will be used to execute sst on disabled heads, in the form:

cpualloc.test n, Where n is the CPU to be tested.

This will force execution of SST on the effected NSP and NVP and indicate whether the test passed, or failed.

It is also possible to power the indicated head off and replace and execute diaginit on the replaced head while the system is in OS.

Al,

3.30.4 ConvexOs 10.0 Crashdump Hang with HiPPI

It has been determined that the crashdump utility in 10.0 ConvexOS will hang with HiPPI installed in the system. This is not a HiPPI problem, but appears to be caused by the crashdump utility, itself.

As temporary solution to the problem, it is recommended that the HiPPI entry be commented out of the /ioconfig file, before attempting a crashdump. Once the hang has been encountered it will be too late to make the necessary changes.
Al,

3.30.5 C3800 System Crashes Less Memory Boards than CPU's

It should be understood that it is possible to generate a crash on a 3800 when attempting to execute code on a system with more cpu's installed than memory boards. This can occur because of problems with Hitachi DRAMS and will occur on an individual memory board if, even one of these DRAM's is installed on a NMC.

The crash that will be encountered is a rdedc hard error. An example of this will appear below.

```
HARDERROR #   BOARD TYPE   PORT/SIDE   EXTRACTOR
-----------   ----------   ---------   ---------
  0           MB_TYPE      4           mb_odd_bank_rdedc_multi_bit_err
-------------------------------------------------------------------
ODD side 'bank_rdedc_multi_bit_err' detected in RDEDC of MB4
-------------------------------------------------------------------
MULTI-BIT error in BCGA BANK3 ( => BANK 8o) detected by RDEDC during
READ operation.
```

This error will be encountered most often when executing code on multiple cpu's and one memory module on line.

Al,

3.30.6 Status of Fuji Poly

It has been decided that the idea of replacing the fuji poly material used on epont connectors, with ecpi will not take place.

The reason for this decision is based on the act that the fuji poly's performance has improved and the ecpi has been found to be of inconsistent quality.

There is no further testing of ecpi being conducted and therefore this should be considered final.

Al,

3.30.7 C3800 spu4000 Faults

The following are C3800 nets recently reported by manufacturing as not being detectable by spu4000.

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1. spu4000 passed but sys_con detected the following:
   ia8_xs1e.wr_data[31..0] to reg xs1e:wr_data_is8 = 0x200000 (expect 0x0)

2. spu4000 missed these shorts that xc_con found;
   ERROR: XC_IA8.TRAP_VECT<7..0> to register ia8:xbi_ncu_intvec_7_0 = 0x57 (expect 0x55)
   ERROR: XC_IA8.TRAP_VECT<7..0> to register ia8:xbi_ncu_intvec_7_0 = 0xae (expect 0xaa)

3. Spu4000 did not detect the following shorts that were reported during ConveOS boot.
   VP6.3_414 (SP0VP0DATA35) VP6.3_314 (VP0SP0DATA35)

These problems will be corrected with the Diagnostics 3.0 release.

Jerry

3.31.1 C3800 Power Transformer Specification

It has been decided that CONVEX will no longer insist on the CONVEX supplied transformer's use with C3800 installations. This more lenient policy is spelled out below and originates from the CONVEX mechanical engineering organization.

As usual, if there are any questions, please contact Hardware Support.

C3800 AC Power Source Specification

This is a brief discussion of the use of alternate power source equipment by Convex C3800 customers. This is not intended to replace the existing site preparation guide, but rather to supplement the guide until this new information can be incorporated into it.

The C3800 power system was designed utilizing a Convex specified power isolation transformer as a front end. The low pass filter characteristics and balanced impedance of the Convex isolation transformer were designed in as a part of the CPU power system to give superior noise immunity and phase balance performance. The system was developed and tested around this specific equipment which can be provided to each customer by Convex to help ensure performance comparable to machines located at the Convex facility.

Convex's position on the use of alternate power sources is now open as long as certain requirements are met. This was not originally Convex's position since all the original emission and immunity tests were performed at the primary of the Convex transformer, requiring its usage. Since that time, more testing has occurred confirming that most any high quality transformer or PDU can perform the required isolation and attenuation functions.

Convex installation documentation is very specific about the C3800 CPU complex being power isolated from all other equipment with an isolation transformer. This isolation not only protects the machine from noise and surges but other site equipment from any surges generated by the Convex equipment. Even Convex peripherals are not allowed on the same transformer secondary.

The use of alternate transformer equipment should meet the following general criteria. The requirement for isolated power dedicated to the C3800 CPU complex does not change with alternate equipment usage.

PERFORMANCE CHARACTERISTICS OF EXISTING OR NEWLY PURCHASED PDU EQUIPMENT -

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The PDU output must be fully isolated and dedicated to C3800 CPU complex only. (Connection of Convex SPU workstation allowed)

The PDU must be at least 50KVA capacity with a minimum K factor of 7 to handle the fundamental and harmonic currents.

The PDU must meet all local codes of the install site for performance and safety.

The PDU must provide a separate 60 Amp circuit to each of up to five C3800 computer bays. (Present connections require 5100C9W or 5100R9W receptacles available from Hubble, Mennekes, or Convex. Future machines will switch to a SP560C9 or SP560R9 connector. Customers will be informed of such a change in advance of site preparation. 5100 plugged equipment will be available on future expansion equipment delivered to sites already prepared with such connectors)

The PDU must be located within 100 feet of the Convex C3800. Outlets from the PDU must be within 10 feet of the Convex C3800.

The maximum main breaker on the input to the PDU must not exceed 125% of the PDU tagged rating.

The isolation transformer within the PDU shall provide full isolation and have a maximum effective coupling capacitance between primary and secondary of 33 picofarads.

Attenuation of line noise and transients shall equal or exceed the following limits at full load and unity power factor:

A) COMMON MODE
0 to 1.5KHZ - 120DB; 1.5KHZ to 10KHZ - 115DB; 10KHZ to 100KHZ - 110DB;
100KHZ to 1MHZ - 60DB.

B) TRANSVERSE MODE
1.5KHZ to 10KHZ - 60DB; 10KHZ to 100KHZ - 62DB; 100KHZ to 1MHZ - 56DB.

The PDU is to provide surge protection such that output surge levels do not exceed IEEE 587 category A levels.

Al,

3.31.2 C3800 Board Revisions

This is intended to explain some new board respins and board revisions on the 3800 that have been reported in other documentation. This is not intended to indicate the availability of these components, but only to inform the field of changes to be applied in the future.

XCL2

This respin will allow for the logging of soft errors with new purge rams available on the 8247 rev H NSP. This capability will not be available on current NSP's and will not be available before Q4.

There will be no retrofit in the field.

XCL1 and XCL2 will be interchangeable.

NMB2/BCGA3/60ns DRAM/NMBPP2

Increases memory performance and allows use of 1/4 populated NMC. Allows 128Mb memory capacity without 1Mb Dram.

NMB2 and BCGA3 required for performance increase.

When using NMB2's with NMB1's no performance increase possible.

New parts cannot be used on existing NMB's. No retrofit for the field. Use current NMB's until exhausted.

Not available before 93.

XDS2 Gate Arrays

Resident on the NIA. Allows for interleaving to be tuned for faster performance when installed with 8247 and 9247 NSP's.

No field upgrade. Not available before Q4

Referred to as NIA2.

8247 NSP

This board is a total respin with the respun gate arrays (NDP, NUS2, NPA) which is to allow the handling of purge ram soft errors.

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This board will work in conjunction with the XCL2.

Available in Q4. NO field upgrade.

9247 NSP
This is a 6247 NSP with the new gate arrays, as indicated above, installed. However, the soft error handling is still kludged on the board itself and therefore this board will not function with XCL2's.

This NSP will generate soft errors for all purge rams except the instr_valid.

No field upgrade.

Al,

3.31.3 Restarting a C3800 After a Crash

It has been found that in order to cleanup properly, after a crash, it is generally necessary to issue 3 consecutive cleanup commands, followed by a "sysreset -s". This is required to avoid problems with automated scripts, such as the auto-reboot script.

The procedure would appear as follows:

```
osclean
cleanup
cleanup
cleanup
sysreset -s
```

This should be taken into account any time it is necessary to recover after a system crash.

Al,

3.31.4 STRAM and Purge Ram Failure hard_logger Messages

The following error will accompany any STRAM, or purge ram failure that is reported by the C3800 hard_logger. This error should be ignored, unless it occurs by itself. The other hard errors should be considered the root cause of the crash.

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In addition to this "tag along" error, it will also be noticed that hard_err2 will generally contain a 00000041, which indicates that both even and odd crossbar return boards are reporting the failure. As can be seen below the erroneous failure is reported by the Return Control gate array.

The rev K NSP will eliminate this "tag along" nuisance.

```
-----------------------------------------------------------------
HARDERROR #    BOARD TYPE       PORT/SIDE    EXTRACTOR
-----------    ----------       ---------    ---------
    0          SP_TYPE             1         sp_nrc.sal_miss3_stop_in
=================================================================
 spl:nrc0.par_err_stop_in = 1 \
 spl:nrc1.par_err_stop_in = 1 | These should all have the same value
 spl:nrc2.par_err_stop_in = 1 /
     Parity error script for
   sal_miss1 bus received by NRC0, NRC1, and NRC2 gate arrays.
   Register name      Ring value              Board signal name
-------------------------------------------------------------------------
   sal_miss3<>      00 06 cc 68              SA1_MISS1<31..3>:SA1_ADDR2<2..0>
   sal_miss3<>       1  1  1  1*             SA1_ADDR2_PAR<0..3>
   * indicates parity error
+++>
<Wed Jul 29 13:32:07 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349):logmsg: General purpose event
Source: sp_nrc_sal_miss3_stop_in
@extractor=sp_nrc_sal_miss3_stop_in @board_type=sp @port=1
****
```

Al,

3.31.5 C3800 Utilities

This includes a list of 48 basic utilities to be used and understood with the C3800. Nearly, every one of these utilities are discussed in the C3800 Troubleshooting Hints Guide. It is recommended that all Fe's with 3800 responsibilities, review this list and insure familiarization with all on the list, before they are needed.

If there are any questions concerning any of these utilities, please contact the TAC.

.....continued on next page.....

System Init Utilities

diaginit	sys_shutdown	cleanup
errintd	mminit	sysrese
initall	abd	

Error Analysis Tools

rslog	hard_err1	hard_err2
xbar_err	nmb_errs	dump_swip
dump_swis	display_log	dump_soft_log
hard_logger	nsp_haz	hang
icach	dcach	ptecach
rcque	mam	

Database Utilities

copmod	cop	cop contents
cdb_browser	fw_rev_update	ucode_rev_update
xsys_config	osc_update	diag_rev_update

Power Tools

pwr_util	powermon	powerdown
cpualloc		

Diagnostics

pb_walk	idc_con	ncutestall
sys_con	xbinteg	xc_con
sst	cpucti	xdiag
mtst		

Al,

3.31.6 C3800 Registers

This is a list of all C3800 registers that are accessible through the SPU interface. These registers can be accessed from a dsh window with a "get".

Most of these registers are not writable, but for those that are, this is accomplished from dsh with a "put".

```
swis_bsrc_msb          swip_bsrc_lsb          swip_bsrc_msb
swis_force_par_err     swip_force_par_err     swis_misc
swip_misc              swis_int_level_ctl     swip_int_level_ctl
swis_int_stat          swip_int_stat          swis_int_ena

swip_int_ena           swis_force_int         swip_force_int
key_switch             nwi_data_loop_back     ncu_addr_loop_back
swis_master_ena        swip_master_ena        swis_fpga_reset
swip_fpga_reset        swis_prog0             swis_prog1
swip_prog0             swip_prog1             swip_prog2
swip_prog3             uart_model             uart_mode2
uart_stat

uart_clk_sel           uart_cmd               uart_rx_hld
uart_tx_hld            uart_input_chng        uart_aux_cntl
uart_int_stat          uart_int_mask          init_uart_cnt_msw
uart_cnt_msw

init_uart_cnt_lsw      uart_cnt_lsw           uart_input_port
uart_output_cfg        uart_start_cnt         uart_stop_cnt
ncu_misc_test_cntl     ncu_xfer_cnt           main_mem_addr
mem_test_even          mem_test_odd           ncu_data_loop_back
mach_serial_number     sys_int_vec            ncu_int_stat
ncu_int_ena            ncu_err_log            clk_cmd_stat
cmd_ena1               cmd_ena2               clk_freq_cnt11
clk_freq_cnt12         clk_freq_cnt13         dis_clk1
dis_clk2               init_burst_cnt_msw     init_burst_cnt_lsw
osc_freq               phase_mon              burst_cnt_msw
burst_cnt_lsw          scn_cmd_stat           err_loc
scn_cnt                io_addr                scn_out_buf
scn_in_buf             scn_mask_buf           scn_comp_buf
soft_log_ccu_cntl      scalar_halt            scn_cntl_ena1
scn_cntl_ena2          hard_err1              hard_err2
hard_err_mask1         hard_err_mask2         run_ena1
run_ena2               nmb_cntl_stat          read_rbe_count
clk_cmd_shdw           scan_mem_err_log       hw_hung
```

Al,

3.31.7 I/O Site Preparation Guide Error

Table 4-8 on page 4-7 lists the Hubbel plug style for the MTD-203 9-Track (200 ips) tape drive as a 5342I. This is in error. It should read 2320.

This same error exists for the MTD-303 on the same table.

Jerry

3.31.8 New System Console Terminal and Cables

There is a new replacement terminal being shipped as the system console. This is the LINK model MC5. This terminal requires new cables for the terminal to spu and terminal to screen printer.

The part numbers for the cables are

System to Terminal: 604-100117-003
Terminal to Printer: 604-080007-001

* Dave Muir *

3.31.9 V5.1 CPU Diag and V1.1 IO Diag Problem

There is a compatibility problem with the V5.1 diag release and the V1.1 IO diag release for C3200 systems.

There are scripts on the SPU in the /hw/field/ptests directory that execute idc4000. This test does not exist on the V1.1 tape and will cause an error when run from the install script. The test has been replaced with idc4010 and it is compatible with idc4000.

Thanks to Mark Jones for this information

* Dave Muir *

3.32.1 C34xx SPU Disk Requirements

All C34xx(Javelin) systems have shipped with a 500MB SPU disk. Should you need to replace this disk, with either a new drive, or an RDS based SPU, you must ensure that the replacement drive is a 500MB one. Failure to do this will cause problems should you ever need to build, or rebuild, the SPU's file systems from tape.

-Kelvyn

3.32.2 C3800 IA/SP Soft Error Logging

Currently IA and SP soft errors are recorded only on the console screen and in the display_log. So, if you are not setting in from of the console when one of these soft errors occur, the only way you will be aware of this occurrence is by reviewing the display_log.

This problem will be corrected in the diagnostic release after Beta 3.0. At that time you can retrieve the information with a "dump_soft_log".

Jerry

3.32.3 C3800 spu4000 Bug

If the scalar boards in a C3800 system are revH or later, there's a known problem with the diagnostic when all installed processors are running st 810 at the same time. It shows up as a vp-sp hard error failure.

If the heads are run separately the error will not show up, if that's what the problem is.

Here's an example of the known failure: Running Vector Processor 0 to XCL Test.

```
+++> <Thu Jul 30 14:52:30 1992> /diag/test/spu/spu4000:../vp_xcl_test.c:273
Subtest Fail (DiagER466): Spu4000 Error: Connectivity Test Failure
Detected Short or Stuck-at-1
Source Signal: VP_SP.HARD_ERROR                    Source Port: 0
Sink Signal: VP_SP.HARD_ERROR                      Sink Port: 1
Sink Field: xcls:CU_TRAP_COMP_SPX
Failing Bit Position:  0
Expected:              00000000
Actual:                00000001
****
```

Jerry

3.32.4 C3800 Auto Reboot

It should be understood that when selecting the network option during installation of the auto reboot daemon, on 3800's, the system is exposed to potential random reboots caused by network related failures.

The failures will generally appear as a system reboot for no apparent reason, which after much investigation, generally leads to a network fault.

Because of this possible problem, it is recommended that the response to the network option in the install script, be answered no. The specific question is:

Do you want ADB to ping $host to see if it is up (yes or no)?

The default of ABD is to monitor the processes over the SWIP/NCU link. This is sufficient to reboot on hangs and crashes.
Al,

3.32.5 C3800 Memory Errors

As reported in a previous tech bulletin, the error shown below can be expected to occur on NMB's with Hitach Drams installed and the system configured with more processors than memory boards installed.

The problem has been identified as a timing problem and is fixed on 1246 NMB's assembly rev B. The solution is to gate the data through an additional register, which is enough to overcome the timing difficulty.

The failure is not severe enough to justify a field upgrade, but all NMB's returned to Dallas will be upgraded during the repair process.

```
 HARDERROR #     BOARD TYPE        PORT/SIDE       EXTRACTOR
 -----------     ----------        ---------       ---------
     0             MB_TYPE            4
mb_odd_bank_rdedc_multi_bit_err
-------------------------------------------------------------
-------------------------------------------------------------
ODD side 'bank_rdedc_multi_bit_err' detected in RDEDC of MB4
-------------------------------------------------------------
MULTI-BIT error in BCGA BANK3 ( => BANK 8o) detected by
RDEDC during READ operation.
```

Al,

3.25.6 Identifying STRAM and PRAM Failures

There has been some confusion in identifying stram and pram failures. In particular, because of the similar extractor names there has been some difficulty in differentiating between pram and stram failures. This document is intended to clarify some of this confusion.

Although these are very basic examples, they should illustrate the difference between the two components.

As STRAM's are utilized in system cache's, tags and scratch rams, therefore these failures will involve data fields ranging from 16 to 64 bits, as can be seen in examples 1 and 3 below:

Purge rams, on the other hand are used for cache housekeeping, updates and validity. So the data fields involved in this are much smaller.

As can be seen from these two examples, both hard errors indicate various size data fields.

The purge ram failures are displayed in examples 2, 4 and 5. As can be seen from these examples, the purge rams consist of 2 bit data fields, in this case <1..0>.

```
EXAMPLE 1
---------
------------------------------------------------------------------
HARDERROR #      BOARD TYPE        PORT/SIDE   EXTRACTOR
-----------      ----------        ---------   ---------
    1             SP_TYPE             0        sp_npar.inst_tag_par_err
==================================================================
 sp0:npar.inst_tag_par_err = 01
     Parity error script for parser_inst_tag received by NPAR gate array
       Ram Address = 7b5    INST_CACHE_ADDR<13..3>
   Ram value           Board signal name
   ------------------------------------------------------
   Ring     00  01  80      PARSER_INST_TAG<31..14>:zero<13..8>
            1   1*  0       PARSER_INST_TAG<32..34>
   Ram      00  09  80
            1   1   0
   * indicates parity error
+++>
<Thu Jun 25 22:06:38 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: sp_npar_inst_tag_par_err
@extractor=sp_npar_inst_tag_par_err @board_type=sp @port=0 ****
```

.....continued on next page.....

```
EXAMPLE 2
---------
------------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE        EXTRACTOR
-----------     ----------          ---------        ---------
    1            SP_TYPE               2             sp_npa0.pval_par_err
========================================================================
 sp2:npa0.pval_par_err = 1
     Parity error script for prd_val0 received by NPA0 gate array
       Ram Address = 636    SA0<22..12>
   Source      Value         Board signal name
   ----------------------------------------
   Ring        1*      PRD_VAL0<1..0>
   Ram         1*
   * indicates parity error
+++>

****

EXAMPLE 3
---------
------------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    1            SP_TYPE               6          sp_npar.que_par_err
========================================================================
 sp6:npar.que_par_err = 01
     Parity error script for icac_data_out received by NPAR gate array
       Ram Address = 781    INST_CACHE_ADDR<13..3>
   Source                  Value                      Board signal name
   ------------------------------------------------------------------------
   Ring  14  89  ff  fc  36  39  7f  a8       ICAC_DATA_OUT<63..0>
          1   0   1   1   1   1   1*  0       ICAC_DATA_OUT<64..71>
   Ram   14  89  ff  fc  36  39  ff  a8
          1   0   1   1   1   1   1   0
   * indicates parity error
+++>
```

.....continued on next page.....

```
EXAMPLE 4
---------
------------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE      EXTRACTOR
-----------     ----------          ---------      ---------
    1            SP_TYPE                0          sp_npa1.ctval_par_err
========================================================================
 sp0:npa1.ctval_par_err = 1
     Parity error script for crd_tval1 received by NPA1 gate array
       Ram Address = 49d   SA1<13..3>
   Source     Tvalue         Board signal name
   ---------------------------------------
   Ring       1*      CRD_TVAL1<1..0>
   Ram        1*
   * indicates parity error
+++>
<Wed Jul 22 09:54:17 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: sp_npa1_ctval_par_err
@extractor=sp_npa1_ctval_par_err @board_type=sp @port=0
****

EXAMPLE 5
---------
------------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    1            SP_TYPE                1          sp_ndp1.pmod_par_err
========================================================================
 sp1:ndp1.pmod_par_err = 1
     Parity error script for prd_mod1 received by NDP1 gate array
       Ram Address = 62d   SA1<22..12>
   Source     Value          Board signal name
   ---------------------------------------
   Ring       2*      PRD_MOD1<1..0>
   Ram        2*
   * indicates parity error
+++>
<Wed Aug 5 11:38:51 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: sp_ndp1_pmod_par_err
@extractor=sp_ndp1_pmod_par_err @board_type=sp @port=1
****
```

Al,

3.32.7 C3800 NVRF2 Failures

It should be understood that the "NVRF2" failure is not the only failures related to the yuvc register. In addition there is only one of these type failures that is a known problem and should be ignored. The other failures are legitimate and should be addressed when they occur.

The yuvc register is the source of parity checking for 4 data busses off of the 3 NDP (Data Path Gate arrays). The 3 NDP's are partitioned in such a way as to allow byte rotation without involving multiple gate arrays. This is accomplished by allowing each gate array to handle 3 bits of each byte. For each byte 1 gate array will handle 2 bits of data and 1 bit of parity for that byte.

The four busses involved in the yuvc are:

CRD	Data Cache Read Data
UPD	Data Cache Update
Ybus	The primary SP external Data bus
VX	Vector to Scalar Data bus

The NVRF2 failure involves, only, the VX bus and is generally originates on the Vector board and is finally detected at the yuvc. This failure can sometimes be addressed by rotating vector boards between SP's, but this is not recommended unless encountering multiple VX data parity errors on the same head. An example of this "known" failure appears below:

```
Hard error Summary
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE       PORT/SIDE     EXTRACTOR
-----------     ----------       ---------     ---------
    0            SP_TYPE             0          sp_ndp.yuvc_vx_err
===================================================================
 sp0:ndp0.yuvc_par_err = 4 \
 sp0:ndp1.yuvc_par_err = 4 | These should all have the same value
 sp0:ndp2.yuvc_par_err = 4 /
     Parity error script for Vx bus received by
   NDP0, NDP1, and NDP2 gate arrays.
   Register name      Ring value              Board signal name
-------------------------------------------------------------------------
   vx<>     00  00  80  00  00  00  4e  43    VX_DATA<63..0>
   vx<>      1   1   1*  1   1   1   1   0    VX_PAR<0..7>
   * indicates parity error
+++>
<Tue Jul 28 20:07:56 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: sp_ndp_yuvc_vx_err
@extractor=sp_ndp_yuvc_vx_err @board_type=sp @port=0
****
```

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If the failure involves one of the other 3 busses and is not a VX data parity error than the problem is Scalar in origin and indicates a failure. These faults should be addressed. A couple of examples of these failures can be seen below:

As can be seen by the next example, this error occurs on the UPD bus.

The next error is indicated on the CRD bus and is a STRAM failure. As with the UPD par_err, this problem should not be overlooked, as it is a more serious issue.

```
Hard error Summary
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE       PORT/SIDE       EXTRACTOR
-----------     ----------       ---------       ---------
    2            SP_TYPE             1          sp_ndp.yuvc_upd_err
===================================================================
 sp1:ndp0.yuvc_par_err = 1 \
 sp1:ndp1.yuvc_par_err = 1 | These should all have the same value
 sp1:ndp2.yuvc_par_err = 1 /
     Parity error script for Upd bus received by
   NDP0, NDP1, and NDP2 gate arrays.
   Register name      Ring value             Board signal name
-------------------------------------------------------------------------
   upd<>  00  00  00  00  00  00  00  20   UPD_DATA<63..0>
   upd<>   1   1   1   1   1   1   1   1*  UPD_PAR<0..7>
   * indicates parity error
+++>
<Sat Jun 20 12:22:10 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: sp_ndp_yuvc_upd_err
@extractor=sp_ndp_yuvc_upd_err @board_type=sp @port=1
****

Hard error Summary
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE       PORT/SIDE       EXTRACTOR
-----------     ----------       ---------       ---------
    0            SP_TYPE             1          ndp.yuvc_crd_err
===================================================================
 sp1:ndp0.yuvc_par_err = 1 \
 sp1:ndp1.yuvc_par_err = 1 | These should all have the same value
 sp1:ndp2.yuvc_par_err = 1 /
     Parity error script for Ybus, Upd, Vx, and Crd buses received by
   NDP0, NDP1, and NDP2 gate arrays.
```

.....continued on next page.....

```
   Register name      Ring value              Board signal name
-------------------------------------------------------------------------
   ybus<>  00  00  00  70  0f  22  c0  00   YBUS_DATA<63..0>
   ybus<>   1   1   1   0   1   1   1   1   YBUS_PAR<0..7>
   upd<>   20  00  0b  10  20  00  3b  17   UPD_DATA<63..0>
   upd<>    0   1   0   0   0   1   0   1   UPD_PAR<0..7>
   vx<>    00  00  00  00  00  00  80  00   VX_DATA<63..0>
   vx<>     1   1   1   1   1   1   1   1   VX_PAR<0..7>
   crd<>   00  00  00  01  22  f0  35  c6   CRD_DATA0<31..0>
/CRD_DATA1<31..0>
   crd<>    1   1   1   0   1   1   1  *1
CRD_DATA0<32..35/CRD_DATA1<32..35>
   * indicates parity error
-------------------------------------------------------------------
```

As mentioned in previous bulletins, the NVRF2 failure is being pursued and will be solved. But, until that time it is important to be able to distinguish this failure from other errors, reported by the same mechanism.

Al,

3.32.8 C3800 Site Prep Guide Power

The "C3800 Site Preparation Guide" lists power requirement for individual components in table 1-14 thru 1-17. These values were theoretical in nature, when released. Below is listed the actual measured values for these components.

COMPONENT	WATTS
Central Cabinet	1200
I/O Bay Cabinet	1200
NIA	1050
NCU	950
CCU	200
CCU BPS	100
CPU Bay Cabinet	1200
NMB	1200
CPU (VP and SP)	2000

.....continued on next page.....

These values are all maximums and individual configuration values do not exist. For example, there is no information available on power dissipation of NMB's of different sizes. So, as these figures are maximum, it is recommended that these figures be used for all configurations.

Al,

3.33.1 Link Terminal Cable PN Correction

There is a typo in bulletin V3W31 article 3.31.9 which identifies the part number of one of the Link terminal cables.

The part number is 604-100117-003 it should be 604-100017-003

* Dave Muir *

3.34.1 C3800 Kernel Damage During a Virgin Install

The C3800 has proven vulnerable to kernel damage occurring during a virgin install of the OS. Even though the problems have only been associated with a virgin install, so far, this problem should be considered after any sysgen that is accomplished on the system.

This appears to be a 3800 problem, only, and has not been duplicated on any other system type.

The symptoms are that the fortran compiler will intermittently abort with the following error:

```
Compiler abort/assert may have been caused by source on 159.7.
fc: /usr/convex/fskel was terminated by signal 'SIGILL'
```

By intermittent, I mean that the compile will fail 60-70% of the time. This failure will occur on all source files and will always report on the same line for each source. The above example indicates that the failure occurred on line 159. The error is occurring with fskel and is an illegal instruction.

Other symptoms associated with this problem are as follow:

1) Disabling the dcache will cause the situation to improve drastically
2) The problem will improve as the physical memory size is reduced
3) There is no head configuration that will affect the situation

It appears that the problem is generated during a sysgen and involves damage to the kernel itself.

The solution to the problem is somewhat painful and involves, first, attempting to move the effected file system (both root and usr) to another disk. This can be accomplished by a cpall, or a dump piped to the restore command.

If this fails to resolve the problem, then it will be necessary to perform a virgin install of the OS.

Al,

3.34.2 New NSP's Fail With Version 2.0 Diagnostics

It has been discovered that newly upgraded NSP's will not function in a field system, running on 2.0 Diags.

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The reason for this is related to two (2) extra fields generated by the 3.0 version of copmod. These two extra 32 bit fields are not recognized by the 2.0 diagnostics. All boards in house are now copped with 3.0, so this affects all boards, now being shipped.

The solution to the problem is to, immediately, upgrade all C3800's to 3.0 diagnostics and 10.2 OS. In addition, at the same time, it is recommended that the backplane upgrade (FMI 93) be performed at this time. This is recommended in order to avoid any other hidden problems.

It is important that both 3.0 and 10.2 be loaded together, as loading 3.0 alone can result in hangs, due to APR problems. In an emergency, this interdependency can be circumvented by enabling the xsys_config entry "enable_cpu_harderrs". This entry is located at the bottom of the xsys_config display. If on then APR is defeated, if off then APR is enabled. It is controlled by the mouse.

It should be understood that it will not be possible to install any replacement boards, until this is accomplished.

For more details on APR, please refer to the tech bulletin, issued on that subject.

It is urgent that this be accomplished, immediately. Please, don't get caught in a situation where this is necessary after the system fails.

Al,

3.34.3 nvrf2 Crash Troubleshooting

It is recommended that after the occurrence of the second nvrf2 crash, on a C3800, that the NVP be rotated between heads. Once this error has shown itself to be repetitive on a specific head is necessary to separate the NVP and NSP for troubleshooting purposes and because some of the causes of the failure are believed timing related. It is recommend that the NVP be the board that is moved because the NVP is more robust and presents less risk in the move.

In many cases, the simple act of breaking up the NSP and NVP have resulted in a solution to the problem.

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Below is an example of the failure that is being referred to:

```
detected_harderrors[0] = 02000000 detected_harderrors[1] = 00000041
enabled_harderrors[0] = 3f005000 enabled_harderrors[1] = 0000007f
****
Extractor Name:   xrt.rtn_par_err_sp6
Port:  0
------------------------------------------------------------------
HARDERROR # BOARD TYPE PORT/SIDE EXTRACTOR
---------- ---------- --------- ---------
0 SP_TYPE 6 ndp.yuvc_vx_err
==================================================================
 sp6:ndp0.yuvc_par_err = 2 \
 sp6:ndp1.yuvc_par_err = 2 | These should all have the same value
 sp6:ndp2.yuvc_par_err = 2 /
     Parity error script for Vx bus received by
   NDP0, NDP1, and NDP2 gate arrays.
   Register name      Ring value              Board signal name
------------------------------------------------------------------------------
   vx<>     00  00  00  00  00  04  00  00    VX_DATA<63..0>
   vx<>      1   1   1   1   1   1*  1   1    VX_PAR<0..7>
   * indicates parity error
```

Al,

3.34.4 Displaying C3800 Memory Soft Errors

As reported in past tech bulletins, the proper utility to display memory soft errors is "dump_soft_-log". To review this, please read article 6, of chapter 8 in the "C3800 Troubleshooting Hints".

To complement this utility,there is a cleaning utility for removing these soft errors. This utility is /diag/hw/soft_clean. This will remove all soft memory errors and reset the pointers for dump_soft_-log.

Al,

3.34.5 Criteria for C3800 Board Replacement

The following guidelines are currently being used to determine replacement of boards in the field. They are listed here to familiarize the field with these guidelines and is not intended for the field to make their own determinations in the matter of replacement.

.....continued on next page.....

1) On the first occurrence of a STRAM. These component failures are generally indications of a failed part and so will be considered for immediate replacement.

2) On the occupance of 2 successive purge ram failures, indicating the same ram and the same address within the ram.

3) Three, apparently, unrelated failures on the same NSP.

4) The occurrence a nvrf2 on either NSP, or NVP, after the boards have been separated. A board will not be replaced until there is evidence that it has followed a moved board. The part replaced, in this instance, will generally be a NVP.

5) Most other failures will be considered a hard failure and result in replacement as warranted.

Al,

3.34.6 Installing 10.0 OS With Sysgened Software

Currently, with 10.0 OS, it is not possible to install sysgened software products on any CONVEX systems, after installing Secure NFS, on a virgin install. This is because that the install script for Secure NFS differs from the install scripts of the other products.

It is possible to work around the problem by editing the most current build file under /sys/sysgen. This file would have the name of the most current sysgen accomplished; for example REL_C2.SECURE.

The underlying problem is that Secure uses spaces for the Source entry and the other install scripts use tabs.

The solution is to edit the source line in this file, which will read:

```
source    yes
```

This line should be changed to "source no" using tabs. An example of the correct entry can be seen below:

.....continued on next page.....

```
machine         c3
cpu             "C-3"
ident           rel_c3
maxmemsize      512
spus            opus5120,c34

options
NFS,NFSCLIENT,SECURE_NFS,TRACE,ASSYMTRACE,INET,QUOTA,UNET,_ACL,_AUD
IT,Secure Ware

pseudo-device   nfs 1
pseudo-device   inet 1
pseudo-device   loop 1
pseudo-device   ether 8
pseudo-device   nc 1
pseudo-device   unet 64
source    no    *****NOTE***** It is important that tabs be used on this line rather than spaces
```

This problem should be resolved in 10.1 OS.

Again, this problem will only be seen on a virgin install and will not occur after this file has been corrected initially.

Al,

3.34.7 C3800 APR

As explained in article 3 of Chapter 8, in the C3800 Troubleshooting Hints, APR (Automatic Processor Recovery) has been introduced with the release of 10.2 OS and 3.0 Diags. With this release will be some new utilities, as well as changes to existing utilities, to support this capability. Please review this article along with the previous document for the most thorough understanding of this subject.

The command 'cdb_get' can be used to retrieve keyword info from the configuration data base. For example, a 'cdb_get dynamic_cpu_harderrs_0' will retrieve this entry. As stated in the other document, a 1 in this register indicates that APR is enabled on that head. The command cdb_get does not accept wild cards and will only display one entry at a time. A more convenient tool would be cdb_browser and query for an entry like dynam* which would return all 8 entries.

.....continued on next page.....

The utility 'diaginit' will now check the assembly rev of the board and the backplane to insure that the head is APR capable. If the rev of the NSP is above H, or greater and the rev of the backplane is B, or greater, then diaginit will set the dynamic_cpu_harderrs entry for that head to a 1.

*****NOTE***** If the backplane is not copped (FMI 93) then diaginit will set the dynamic_cpu_harderrs to 0 and thus prevent APR functionality.

The 'cpualloc' utility now works to enable and disable a head online. This utility has 2 switches; -d which will disable a head and -e which will enable the head. For example:'cpualloc -e 0' will enable and download ucode to head 0. This utility is a SPU level function.

The utility 'cpuconf' has been around for a while and has been used to remove a head from the scheduler at the OS level. Now 'cpuconf' calls cpualloc to allow physical removal and replacement of a head in OS. This utility utilizes the sam switches as cpualloc.

A new utility is available on the spu for running sst against the specific head. This utility is 'cpualloc.test' and when followed by a cpuid will execute SST against the NSP and NVP in the specified head. This will allow a shortcut method to execute SST on the head, rather than having to run through the menus and setup.

The entry 'enable_cpu_harderrs' is used to override, or allow APR to function. Although this is an entry in the cdb, a switch is provided in the xsys_config display for setting this entry. When on APR will not function, regardless what other registers indicate. For operation, this entry should be left off in xsys_config.

As a reminder APR will not function with a single head enabled.

It will be possible to execute 'cpuconf -d n' on a specific head to remove it from the complex and then execute 'spucmd /diag/hw/cpualloc.test n' to run SST on the entire head. It would, also, then be possible to run additional diagnostics, or return the head to the complex with 'cpuconf'. It is recommended that the system, or head be in a quiescent state before attempting to remove it from the complex.

Al,

3.34.8 PPC and BPC Failures - EEPROM Not Write Protected

It has been discovered that PPC's and BPC's are vulnerable to catastrophic failure. The reason is because the EEPROM's on these devices are not write protected and so can be written to accidentally. Although this is a real possibility, it has only been witnessed 3 times in a field environment.

The symptoms exhibited, when this happens, is that an individual board, or single bay will power down during operation, for no apparent reason. It will then be impossible to power this particular failed component up again.

*****NOTE***** Boards that power down, but come right back up are not included in this situation.

If this particular situation occurs on a system, it is recommended that the firmware be downloaded by pwr_util. If it is the write protect failure, then this will clear the problem. Replacing the PPC, or BPC will also correct the problem, but download of firmware is far quicker and cheaper.

If this should occur, please contact the TAC.

This problem is being address and a solution, a new loader, will be released in 3.1 of the diagnostics. This loader will allow the write protection of these EEPROM's.

Al,

3.35.1 C3800 APR Information

It should be understood that, in addition to being able to run diags on a single head with the rest of a 3800 in OS, APR will allow the head to be removed and replaced without bringing the system down.

It is perfectly acceptable to execute diaginit while the system is up. This will only affect the head that has been removed and will have no impact on the remainder of the complex.

The only restriction is that only one process can be performed on the downed head at any one time. Otherwise it is possible to execute any cpu diagnostics, or SST, or cpualloc for download of micro-code. An initall, or mminit cannot be performed, as these utilities are not restricted to a specific head.

It should further be understood that APR and options are a boot time parameter and cannot be changed on the fly.

In addition, it is possible for APR to fail in the act of sorting out the failure mode and thus be able to clear the error. This situation can result in a crash, but the head will still be removed from the complex. This means the system will reboot short one head. To counter this possibility it is recommended that the system be checked for available heads when rebooting.

This scenario will, also, take place after a fatal CONVEX Unix Error.

This problem has been reported and will be fixed in the Diag release 3.1.

Al,

3.35.2 Diagnosing NMB Failures

Memory related input staging register failures are reasonably easy to fix if it's first understood and the proper approach is utilized.

First it should be understood that the Input staging register is the first place in the data path of the NMB that the parity is checked. With this in mind, it is easy to understand that a parity error at this point generally indicates a failure external to the memory board itself.

An example of this type of error can be seen below:

.....continued on next page.....

```
------------------------------------------------------------------
HARDERROR # BOARD TYPE PORT/SIDE EXTRACTOR -
---------- ---------- --------- ---------
    1          MB_TYPE     0 mb_ise_data_perr
==================================================================
 EVEN side 'ise_data' ctl_par_err detected in discrete input staging
 registers by MB0. Request came from SP0 through the XS<even>.
------------------------------------------------------------------
  PARITY CHECK - The XBAR data is saved in lookaside registers in
                 the XS1 and XS0. This is the data that the XBAR
                 sent to the NMB for this request. Any difference
                 between the XBAR data and the NMB data may indicate
                 a connectivity problem between the XBAR and the NMB.
                 Otherwise the XBAR or the SP-XBAR connection is bad.
------------------------------------------------------------------
      Data                  Scan Field
   ----------------------------------------
    ***Data was not preserved in SP0***
   ----------------------------------------
   ac 00 00 3f     xs1e:wr_data_lsd2[0]<31..0>
    1  1  1  1         xs1e:wr_par_lsd2[0]<0..3>
   ----------------------------------------
   ac 00 01 3f     mbs0:ise_sys.rwre_data<31..0>
    1  1  1* 1         mbs0:ise_sys.rwre_par<0..3>
   ----------------------------------------
   * indicates parity error.
Note that quantities in "<>" delimiters are bit descriptors.
They are not part of the scan field name.
------------------------------------------------------------------
```

This error could have just as easily occur on the odd side with mb_iso_data_perr.

As can be seen from the example, there is a lot of information displayed. The display indicates that the source of the failure is SP0. This is very valid information, except when SP0 is indicated. This is because SP0 is the default and as such will be called out when no other source is available. If the source had been SP1 then this would have been a different situation.

The next, valuable, source of information is the data display for xs1 and mbs0. This data should be evaluated for any differences. As can be seen above, there is a difference between the data exiting the crossbar <xs1e:wr_data_lsd2> and the input to the NMB <mbs0:ise_sys.rwre_data>. The difference being bit 8. This is a definite indication of a connectivity failure between the Xbar and that memory board.

.....continued on next page.....

If no defence exists between the Xbar and memory data, then the utility xbar_err should be used to determine the likely source of the error. In this case if the data had not changed and with SP0 called as the source a likely candidate would be XS1e, or SP0. The xbar-err tool would offer further evidence of this.

In many cases the above hard error will be accompanied by ctl_par_err's, which can generally be ignored and send_par_err's which is displayed below:

```
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    2           XS1_TYPE              0           xs1.send_par_err_mb0
===================================================================
 Send parity error detected by MB0 from SP0 in XS0/1E
        Data                Scan Field
  ----------------------------------------
    ***Data was not preserved in SP0***
  ----------------------------------------
  ac 00 00 3f       xs1e:wr_data_lsd2[0]<31..0>
   1  1  1  1       xs1e:wr_par_lsd2[0]<0..3>
  ----------------------------------------
  ac 00 01 3f       mbs0:ise_sys.rwre_data<31..0>
   1  1  1* 1       mbs0:ise_sys.rwre_par<0..3>
  ----------------------------------------
  * indicates parity error
-------------------------------------------------------------------
 xs1e:m_err_en<0> = 1
 xs1e:send_par_err<0> = 1
+++>
<Wed Apr 29 18:33:56 1992> logmsg:../logmsg.c:56
Hard Error Message from Extractor (DiagER349): logmsg: General purpose event
Source: xs1_send_par_err_mb0
@extractor=xs1_send_par_err_mb0 @board_type=xs1 @port=0
****
```

This error will normally provide supporting evidence of the Input staging register error. The Xbar and memory data registers should indicate the same data as the Input staging error. Additional information will be the xs1e:m_err_en<0> = 1 and the xs1e:send_par_err<0> = 1. These registers should support the hard error indication.

One thing to remember is that when the m_err_en register is set to 1, then the clocks are stopped to XS0 and XS1. This will be confirmed in the xbar_err. The supporting xbar output is shown below:

.....continued on next page.....

```
XBAR Error Logger/Identifier Version 0.7 (some testing done)

Halting System
System clocks halted
   Checking xrte for errors
Error detected by xrte -- board has halted
   Checking xrto for errors
   Checking xs0e and xsle for errors
Error detected by xs0e and xsle -- boards have halted
NMB0 detected parity error on data from NSP0
  Data Par in XBAR: 0x00000000 0x6 ***Parity Error***
  addr= 3fffffc cycle= 0 wr_zone= 0 ctl_par= 10 -No Parity Check-
  Compare with NSP and NMB
  Checking xs0o and xslo for errors
```

Al,

3.35.3 C3800 Pbus Architecture

It should be understood that the Pbus on the C3800 is, architecturally, identical to the Pbus on a C2, so that all characteristics apply to both.

This includes the fact that the x and y ports between vbcu and viop are reversed, as referenced to each other. This means that when moving the x cables to the y side for testing, or vice-versa, it is necessary to rotate the cables. This means that y3 will go to x1 and so-forth.

Al,

3.35.4 C3800 Spu Prompts

There are 2 spu prompts utilized in the C3800 CONVEX_OS window.

There is the standard "spu>" type prompt which indicates that OS is not running on the system and is generally in dshell.

The other prompt, "spu[2]#convexos! indicates that the system is in OS and a ^D will return you to the system OS level. This prompt will change to the standard spu> prompt as soon as the OS is halted; either by a shutdown, or an osclean.

Before attempting a boot to the OS a check of this prompt should be accomplished. It is recommended that this hint be passed to operators to prevent confusion.
Al,

3.35.5 C3800 cop Utility

It should be understood that the utility "cop", on C3800's, does not read, directly, the cop chips, but instead, prints the output of the configuration data base (cdb).

This can cause some confusion, as the the cdb is not updated, except as a result of a power up. This means that after executing copmod, the changes will not be reflected in the cdb until power cycling the system. This means that copmod changes will not, necessarily, appear in the database when first examined.

This should not be interpreted as a failure of the copmod, but as a functional issue with the database.

Al,

3.35.6 PETS V3.0 Known Failures

This is a combined list of known 3.0 related PETS failures. Although many of these appear in other technical bulletins, a comprehensive list of failures should be of benefit:

1) A bug causing wrong answers in prll.009 due to a missing expected answer file. This bug will result in WRONGANS failures with this subtest. (C34XX specific, only evident when running systems script)

2) Screen has a bug caused by an invalid margin sequence for c1. This should be corrected from "u ul" to "uu ul". (C1 Specific)

3) In the script "run48" the goto statement in the C3400 switch statement has a ":". This ":" should be at the actual goto statement for TypeParallel. If not corrected, this will cause the script to exit. (34XX specific)

4) Test 14 and 15 will now indicate that they will not execute. In previous releases these tests would indicate that they were run once and never repeat. The tests are disabled due to conflicts with file system frag sizes greater than 1K.

5) On C3800 systems it will be necessary to comment test.046 out of the scripts and move the module, in the Processes directory, to test046.sav. This is necessary because this test module is defective on the released version. Not removing test.046 from the scripts will result in a core dump.

6) The test.041 is moved for C3800's for much the same reason.

.....continued on next page.....

7) All part1 tests were broken by the new mpa in ConvexOS 10.1. This can be solved by loading the previous mpa utility in PETS/bin and moving PETS/bin before $path in path+aliases.

8) On all systems, it is possible to encounter failures with the run96 script due to the incorrect /bin/csh being installed on the system. The failures exhibited can range from core dumps to the script appearing to start, but cease running after 30-45 minutes. In the latter case, no error indication will be given, but PETS will just die. To get around this problem it is necessary to copy /bin/oldcsh to /bin/csh at single user and return to multi.

9) On C3800's running APR, if a head is removed from the complex, while executing PETS part1, then all subtest will result in coredumps. In addition, when the head is returned to the complex, no tests will be executed on this head until PETS is restarted.

Al,

3.35.7 C3800 SPU Software Restore

Please, keep in mind, when restoring software on the C3800 SPU it is necessary to do so from /. It is very easy to make the mistake of doing a restore from diaguser, as that is where the work station boots to.

If the restore is not done from /, then the user id's will be changed and it will not be possible to boot, or worse.

Al,

3.35.8 io5000 Failure on C3800

It is not possible to execute diagnostic io5000.t on multiple VIOP's when installed in a C3800. This does not apply to any other CONVEX product.

When executing io5000 on more than a single VIOP, the second module will fail when it is booted during subtest 200.

The temporary solution is to execute the io5000 diagnostic on a single VIOP at a time.

Al,

3.35.9 Isolating System Hangs on C3800

The scalar_halt register can be a useful tool in establishing the hardware source of certain system hangs and halted systems, where hard information is lacking.

The scalar_halt register is a 32 bit register contained on the XCL and is used, exclusively to trap the first occurrence of a hard error, by monitoring the stop_cntr and hw_hung signals from each head.

The contents of this register can be examined by means of a "get scalar_halt" at the SPU Prompt.

An example of the returned output is shown below:

```
scalar_halt
VALUE: 16#00000000
|31 |30 |29 |28 # 27 | 26 | 25 | 24 # 23 | 22 | 21 | 20 # 19 | 18 | 17 | 16
|           Reserved                #          SCALAR HW HUNG
|15 |14 |13 |12 # 11 | 10 |  9 |  8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 |  0
|           HALT MASK               #                HALT
```

The HW HUNG field indicates that the specified processor is in a hung state. In other words, not started execution of an instruction in a specified number of clocks. The processor is indicated from right to left, with bit 16 indicating processor 0 and bit 23 for processor 7.

The HALT field is generated from the stop_cntr signal and indicates the specified processor has halted and clocks have been stopped.

Al,

3.35.10 Slipping Sectors With idcfmt

When attempting to do a slip of a bad disk sector using "idcfmt" it is suggested that the filesystem that contains the bad sector be dismounted.

While "idcfmt" contains code to lock the disk during a slip, this cannot be guaranteed as a fail-safe approach to slipping a bad sector on a mounted file-system, and all being well afterwards.

Another suggestion prior to a slip would be to obtain a hard copy of the grown defects list of the disk, just for reference.

-Kelvyn

3.35.11 C3400 Power Supply Test Jumper

There have been several questions on the small jumper assemblies that are shipped with the C3400-XX systems. These jumpers are for power supply adjustments if all boards must be removed from the system to accomplish the adjustment.

The sense cable is removed from each supply and the jumper installed in place of the sense cable. This will enable the supply to energize when the circuit breaker for the individual supply is turned on.

* Dave Muir *

3.35.12 C3480-EX CPU Board Placement

If you reconfigure a C3800-EX with less than 8 heads, it is necessary to have all cpu boards installed in adjacent slots. This is due to a bug in mminit that will not initialize memory correctly if the CPU boards are not in adjacent slots.

This bug exists in Version 1.2 and 1.3 of the CPU Diagnostics/Database. This will be fixed in 1.4 release.

* Dave Muir *

3.35.13 Damage to Gate Arrays on C3400 CPU Boards

Several JCPU's returned from the field have had damage to the 20 mil pitch function unit gate arrays. These are the parts with the extremely small leads. Due to their proximity to the front and side rails, they are extremely vulnerable to handling. A misplaced thumb can easily crush the leads. The part designations in question are 20C1, 39C1, 58C1, 77C1 AND 21X6. The most likely failures as a result of lead damage are function unit hard errors (XBUS and YBUX parity errors).

Please be aware of this potential problem and handle the boards with care.

David Horak
Field Service Test

3.35.14 ESDI Disk Controllers.

All 4 disk ports on the ESDI disk controller (DKD-203, 220-000011-200 or 220-000025-200) can be used under V9.1 with a sysgen and under V10.0 of ConvexOs.

These controllers are used in the C3400-ES for drives installed in the internal disk chassis. They are also used for CONVEX ESDI disk system. This is a rack mount for up to four 5.25" ESDI drives. These can be either 650mb or 1.3gb disk modules. Controller 220-000025-200 is required for the 1.3gb disk modules. This controller can also be used with the 650mb modules.

* Dave Muir *

3.36.1 C3800 diaginit Failure

If you have a diaginit failure with entries in the display_log similar to the following, it is possible that the message queue for diaguser has filled up.

```
+++>
<Mon Aug 31 15:06:30 1992> /diag/bin/bpccommd:../cxmsgsnd.c:40
SW Error (DiagER128): msgsnd(2): operation failed

Line: 539            Source: ../bpccommd.c

Msgqid=0x00000003  Msgp=0xf7fff564  Msgsz=0x00000008  Msgflg=0x00000800
Errno=11
No more processes
****
```

To verify if this is the problem, enter "ipcs -qo" at any spu prompt. If QNUM for diaguser is near maximum (maximum is 99) then the only solution for correcting this problem, at this time, is to reboot the spu. The following is an example of a spu having an excessive number of messages active in the diaguser queue and therefore diaginit could not continue.

```
spu> ipcs -qo
IPC status from flt_7 as of Mon Aug 31 15:18:32 1992
T     ID     KEY        MODE        OWNER    GROUP CBYTES  QNUM
Message Queues:
q      0 0x4c0509c4 -Rrw-rw-rw-      root     wheel      0     0
q      1 0x000000a5 -Rrw-rw-rw-      root     wheel      0     0
q      2 0x00000183 -Rrw-rw-rw-      root     wheel     43     1
q      3 0x420002e3 --rw-rw-rw- diaguser diaguser    792    99
```

The following is an example of a message queue taken while the system was in ConvexOS (Note: the QNUM for diaguser should normally be less than 10).

```
spu> ipcs -qo
IPC status from flt_7 as of Tue Sep 1 13:41:35 1992
T     ID     KEY        MODE        OWNER    GROUP CBYTES  QNUM
Message Queues:
q      0 0x4c0509c4 -Rrw-rw-rw-      root     wheel      0     0
q      1 0x000000a5 -Rrw-rw-rw-      root     wheel      0     0
q      2 0x00000183 -Rrw-rw-rw-      root     wheel      0     0
q      3 0x420002e3 -Rrw-rw-rw- diaguser diaguser      0     0
```

See the ipcs man page for further information. As usual, the diagnostics people are working on this problem.
Jerry

3.36.2 C3800 nag/augat Failure

The following is an example of a nag failure caused by a faulty augat connector. The augat in this example was found to have a partial open on pin 126, section 4 (VP6_SP6.VXA_ADDR<2>.

```
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE    EXTRACTOR
-----------     ----------          ---------    ---------
    0            SP_TYPE               6         sp_nag0.vxaq_par_err
===================================================================
 sp6:nag0.vxaq_par_err = 1
   Parity error script for vxa_addr received by NAG0 gate array.
     vxaq_addr0<15:0>         ff  f8          VXA_ADDR<15..0>
     vxaq_addr0_par<0:1>       1   1*         VXA_ADDR_PAR<2..3>
     vxaq_addr1<15:0>         0a  cc          VXA_ADDR<15..0>
     vxaq_addr1_par<0:1>       1   1          VXA_ADDR_PAR<2..3>
     vxaq_addr2<15:0>         0a  d0          VXA_ADDR<15..0>
     vxaq_addr2_par<0:1>       1   0          VXA_ADDR_PAR<2..3>
     vxaq_rptr_las<1:0>        0              VXAQ_RPTR<1..0>
```

Jerry

3.36.3 C3800 Temperature Sensors

The following is a picture of a powermon on the I/O bay and CPU bay. Below each picture is a listing identifying the temperature sensors in each bay.

```
                              I/O Bay Sensors

                  ------------------ PPC Status --------------------
confg  f/w  pt backplane plt brd brd brd brd brd brd brd brd bay bps bus bus
by pp  rev  id slot type typ -0- -1- -2- -3- -4- -5- -6- -7- pwr num OK  on
0|    ** ***** **
1|    ** ***** **
2|00 00  2.8  08  07 IO_B IA IA                                 00  01  00  00
3|00 00  2.8  08  08 IO_B CU CU                                 00  00  00  00
4|    ** ***** **
5|    ** ***** **
6|00 00  2.8  09  06 XBAR XPB XPB XRT XS1 XS0 XCL XS0 XS1 XRT 00  00  00  00
7|00 00  2.8  08  0c CCUR CCU ERR                              00  01  00  00
```

.....continued on next page.....

```
                  ------------------ Temperature Status --------------------
          --- Status ---          --- Outlet(C) ---        --- Inlet(C) ---
f/w rev   Sensor   BdErr           warm         hot          warm         hot
 2.16       00       00             49          63            49          63
Temp Sensors:     1        2        3        4        5        6        7        8
    Status:      OK       OK       OK       OK       OK       OK       OK       OK
   Temp(C):      30       10       10       10       25       25       10       10
Fan Sensors:      0        1        2
    Status:      OK       OK       OK
     Value:      00       00       00

Temp sensor 1 - in xbar outlet near central cabinet.
Temp sensor 2 - Left ccu sensor.
Temp sensor 3 - Bay4 outlet - in blower cage.
Temp sensor 4 - Right ccu sensor.
Temp sensor 5 - in xbar inlet in front of door fans.
Temp sensor 6 - Intake (directly below and in front of boards).
Temp sensor 7 - Not used.
Temp sensor 8 - Not used.
Reading of 10 on temp sensor - sensor most likely disconnected.

-------------------------------------------------------------------------------
                                CPU Bay Sensors

                  ------------------ PPC Status --------------------
confg   f/w   pt backplane plt brd brd brd brd brd brd brd brd bay bps bus bus
by pp   rev   id slot type typ -0- -1- -2- -3- -4- -5- -6- -7- pwr num OK  on
0|    ** ***** **
1|00 00   2.8   00   06  CPUL  MB MB                                 00   00   00   00
2|00 00   2.8   00   07  CPUL  SP SP                                 00   01   00   00
3|00 00   2.8   00   08  CPUL  VP VP                                 00   01   00   00
4|00 00   2.8   01   09  CPUR  VP VP                                 00   04   00   00
5|00 00   2.8   01   0a  CPUR  SP SP                                 00   04   00   00
6|00 00   2.8   01   0b  CPUR  MB MB                                 00   05   00   00
7|    ** ***** **
                  ------------------ Temperature Status --------------------
          --- Status ---          --- Outlet(C) ---        --- Inlet(C) ---
f/w rev   Sensor   BdErr           warm         hot          warm         hot
 3.16       00       00             49          63            49          63
Temp Sensors:     1        2        3        4        5        6        7        8
    Status:      OK       OK       OK       OK       OK       OK       OK       OK
   Temp(C):      10       10       17       10       10       14       10       10
Fan Sensors:      0        1        2
    Status:      OK       OK       OK
     Value:      00       00       00
```

.....continued on next page.....

```
Temp sensor 1 - Not used.
Temp sensor 2 - Not used.
Temp sensor 3 - Bay outlet - in blower cage.
Temp sensor 4 - Not used.
Temp sensor 5 - Not used.
Temp sensor 6 - Intake (directly below and in front of boards).
Temp sensor 7 - Not used.
Temp sensor 8 - Not used.
Reading of 10 on temp sensor - sensor most likely disconnected.
```

Jerry

3.36.4 SCSI Tape Driver Bug

If you have a C3480 or DAT tape sub-system at your accounts, and are seeing the following type of errors, you should obtain the 3480 SCSI driver patch. The patch, 10.2.128, for the SCSI driver is available from the TAC.

```
[SPU @18:06:06] errintd: **** SOFT ERROR DETECTED **** description
follows...
[SPU @18:06:06] PI2[0]: CCU[0] internal hard error.
[SPU @18:06:06] errintd: **** SOFT ERROR DETECTED **** description
follows...
[SPU @18:06:06] PI2[0]: CCU[0] internal hard error.
```

These messages are repeated until the system is shut down or it crashes.

* Dave Muir *

3.36.5 C3400 Systems With Dual PI-2's

C3400 systems with dual PI-2 may experience the following errors:

```
[SPU @01:44:41] CUJ: hard_err is not set
[SPU @01:44:41] PIY/PI2: Hard error detected.
[SPU @01:44:41] PIY/PI2: [#654] interrupt arbitor error
[SPU @01:44:41] PIX/PI2: Hard error detected.
[SPU @01:44:41] PIX/PI2: [#654] interrupt arbitor error
[SPU @01:44:42] CPU0/JCPU: hard_err is not set
[SPU @01:44:42] CPU2/JCPU: hard_err is not set
```

.....continued on next page.....

This may be accompanied by:

```
[SPU @01:44:38] CCU[0]/IDC: Software panic
[SPU @01:44:38] CCU[2]/VIOP: VIOP software induced error
[SPU @01:44:39] CCU[4]/VIOP: VIOP software induced error
[SPU @01:44:39] CCU[5]/VIOP: VIOP software induced error
```

The IOP reported errors may or may not be present with the #654 arbitor error. It is also possible that one or both of the PI-2's will report the error at the same time. This problem is corrected with Revision "D" of the 410-003224-200 PI-2 board.

This problem has been seen only on C3400 systems with dual PI-2's. Revision "D" of the PI-2 will correct ONLY the specific type of errors mentioned above.

* Dave Muir *

3.37.1 Locating C3800 Connectivity Problems

As a refresher for locating connectivity problems off the info contained in spu4000 subtest 810:

The following example will illustrate the current error format of subtest 810:

```
Source Signal: sp_xse.wr_data                    Source Port: 3
Sink Signal:   sp_xse.wr_data                    Sink Port: 3
Sink Field:    xs1e:wr_data_is [3]
Failing Bit Position: 10
Expected:             00000400
Actual:               00000000
```

From the example; the source signal indicates the net in error. The sink signal is used a check on the failing net as the sink should be driven high on the next clock. The net indicates the direction of the signal. In this case the sp is the source with the xse as the termination point. The termination is always found on the second field of the net.

The source port indicates the point of origin for the failure. In the example the net would become sp3_xse.wr_data. The port value will follow physically the configuration of the system. In the case of a value "9" in this location, will mean that the xbar is the source.

The sink field is generally a register location on the board that detected the failure. In this case it is the input staging register on xs1e.

The failing bit position is self explanatory. The expected value is the data pattern expected to be seen by the test and the actual indicates the results. Keep in mind that a 0 value for the failed bit will indicate a open and a 1 value indicates a short. Quite often multiple 1's will be displayed for shorted nets.

Al,

3.37.2 Powering System With the pwr_util

There are certain situations that warrant powering certain areas of the system up without going through the entire diaginit process. This procedure can be followed to circumvent the diaginit and induce the component to complete the power applied process.

.....continued on next page.....

```
a) Bpc chk interlock   b) Reset uart     c) Bpc reset      d) Init bpc
e) Offline bpc         f) F/W revision   g) F/W Download   h) Bay Config chk
i) Cop Read            j) Cop Write      k) Bay Power chk  l) Power On
m) Power Down          n) Send Status    o) Set Voltage    p) Set temp
r) busses off          t) Transparent
q) Quit                ?) Print Menu
```

To reproduce the diaginit process it is necessary to execute the following commands in order:

1) c (Reset the BPC) Assert the reset line on a specified BPC. This forces the set of PPCs connected to this BPC into reset also.

2) d Reinitialize the BPC and force it to look for interlock with its PPCs. This operation is normally done when powering on the system as the first step in establishing communications between SPU and BPCs.

3) h Force the BPC to poll its PPCs and check that the con figuration in the bay associated with this BPC is valid. A block of data, called the bay status message,is reported to the user after this operation which shows the status of the bay and each PPC connected to it. The BPC updates its internal information on the status of each PPC and the BPC environment based on this information.

4) k Force the BPC to poll its PPCs and check that the power supplies in the bay associated with this BPC is valid. A block of data, called the bay status message, is reported to the user after this operation to show the status of the power system. The BPC updates its internal information on the status of each PPC and the BPC environment based on this information

5) l Apply power to a board's busses. This will not bring up a board that has lost its 300 volt supply.

The above procedure will permit a total power configuration of the selected system components.

A status of the powered up components can then be obtained with a "n". This will yield the following display:

.....continued on next page.....

```
PPC Status
  bay pp  fw  prt bkpln bkpln plt bd bd bd bd bd bd bd bd bay bps bus bus
  cnf cnf rev  id slot  type  typ 0  1  2  3  4  5  6  7  pwr num  OK  on
0|ff  ff  ffff ff  ff    ff    ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
1|00  00  0110 00  06    02    01 01 00 00 00 00 00 00 00  00  00  00  00
2|00  00  0110 00  07    02    02 02 00 00 00 00 00 00 00  00  01  00  00
3|00  00  010d 00  08    02    06 06 00 00 00 00 00 00 00  00  01  00  00
4|00  00  0110 01  09    03    06 06 00 00 00 00 00 00 00  00  04  00  00
5|00  00  0110 01  0a    03    02 02 00 00 00 00 00 00 00  00  04  00  00
6|00  00  0110 01  0b    03    01 01 00 00 00 00 00 00 00  00  05  00  00
7|ff  ff  ffff ff  ff    ff    ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
Temperature Status
  f/w rev temp_stat temp_0 temp_1 temp_2 temp_3 temp_4 temp_5 temp_6 temp_7
    0209       00      ff      ff      c1      ff      ff      ae      ff      ff
in_wrm_set in_hot_set out_wrm_set out_hot_set BPC_err fan0 fan1 fan2
    9c          82          47          3a          00      00   00   00
```

Al,

3.37.3 Replacing the Crossbar Backplane

The following procedure can be followed when replacing a crossbar backplane in the field:

1) Remove the crossbar boards (7) and place in static free containers.
2) Remove rear crossbar door.
3) Remove all ribbon cables and other power and sensor connectors from backplane.
4) Remove the card cage. This is attached to the backplane by 8 screws, 4 front and 4 rear.
5) Remove rear xbar airflow sensor.
6) Remove even and odd side xbar power pallets. These are fastened by 2 screws in the rear and one forward.
7) Remove xbar clock cables on the underside of the backplane.
8) Fashion an epont restraining tool. This can be accomplished with twine, or a coat hangar. The purpose is to force the epont connectors to rest just above the backplane.
9) Remove all epont connectors and suspend above backplane with tool.
10) Remove 6 screws holding backplane to cabinet. The two rear screws have no nuts, but the 4 forward screws are held with nuts.
11) Remove backplane by lifting slightly and sliding rearward.
12) Move power pallet mounting plates to new backplane.
13) Clean epont/fuji poly before installing new backplane.
14) Slide new backplane in from rear.
15) Fasten backplane in place with 6 mounting screws.

.....continued on next page.....

16) Re-install epont connectors to backplane, carefully removing restraint tool.
17) Reinstall card cage.
18) Install both power pallets.
19) Install air flow sensor.
20) Install clock cables.
21) Re-install all removed cables from backplane.
22) Re-insert xbar boards.
23) Install rear door.

Al,

3.37.4 Trouble Shooting Crossbar Power Problems

It should be understood that for power configuration purposes, it is possible to remove individual crossbar boards and still apply power to the crossbar.

This procedure can be used when attempting to isolate failures in the power configuration portion of diaginit, that are suspected of being caused by a single board.

This can also be done in isolation of even and odd xbar power pallet failures. Or, to copmod a xbar board which can be accomplished by first entering a "d" under pwr_util and then a "h". This is sufficient to get power to the cop chips, so that copmod can be executed.

Al,

3.37.5 Potential Problems Installing ConvexOs 10.2

The following problems can be encountered when installing 10.2 OS.

- there is a minor misprint in the doc: there is a missing semicolon just in front of "then"
- the entry to start the cpu_monitor daemon should be entered in /etc/rc.local after the 'standard daemons', which are started in /etc/rc.std?
- in the /etc/cpu_monitor.config file is a typo: the line 'SST_REENABLE = 1' should read 'SST_ENABLE = 1'

Achim Hoffmann

3.37.6 C3800 SPU Utilities

As a reminder, it should be understood that nearly all of the standard C3800 SPU level utilities are designed to function under dshell. These utilities will not function if executed from a non-dshell window.

In addition to set paths properly, they should be executed under diaguser.

If attempting to execute these utilities under su, or root, it should be realized that root on the SPU uses bourne shell. This means that these commands and utilities will not function.

Some examples of commands, or utilities that will be affected are the get/put, rslog, xbar_err, nmb_errs, etc.

Al,

3.37.7 Power Pallet Failure

The following power pallet failure is being forwarded as an example to show what other affects power failures can have on the system. In this failure, as can be noted in the WARNING: message below, the voltage busses for this board were turned off. What the message does not tell you is that, in this case, all boards in bay 0 were turned off and diaginit would not power bay 0 back up. The only way this problem could be cleared was to reboot the spu.

As can be seen in the below example, A/D channel 3 reported the failure. The actual problem with this board was found in the power brick slave 5 (A/D channel 3) circuit.

```
**************************************************************************

+++>
<Tue Sep 8 14:12:30 1992>    margin:../set_points.c:97
Env Error (DiagER350): message received by SPU

BPC: 0              BAY: 0
PPC: UNKNOWN        SLOT: UNKNOWN       TARGET: bay0
BPC MSG:     Setpoint command
PPC did not acknowledge command

msgid:20 length:08 source:08 nwi_uart:00 misc0:00 misc1:00 group:78 error:01
****
Operation failed.  Bus veel0k
```

.....continued on next page.....

```
+++>
<Tue Sep 8 14:12:30 1992>     margin:../set_points.c:97
Env Error (DiagER350): message received by SPU

BPC: 0              BAY: 0
PPC: 2              SLOT: 7             TARGET: sp0
PPC MSG:      Voltage error
A/D channel 3 trim failed

msgid:20 length:12 source:02 nwi_uart:00 misc0:0a misc1:0e group:f3 error:23
****
WARNING: this error has caused the firmware to turn off the voltage busses for
this board! You can repower the board with diaginit Operation failed. Bus vttga

*******************************************************************************
```

Jerry

3.37.8 SCSI Driver Problem Revised Information

In V3W36 I reported a fix for a SCSI problem (patch 10.2.128) that corrects a problem with repeated CCU[n] error messages. This patch was only applicable to 10.2 and 10.1 so it could not be applied to 10.0

This problem has been corrected in V10.1.2, which will start shipping to the field on September 15.

Since the revised version of ConvexOs will bee shipping next week, there will not be a patch developed for 10.0 of ConvexOs.

* Dave Muir *

3.38.1 C3800 Running With APR Enabled

It should be understood that on a C3800 running with APR enabled, it is not possible to manually remove a head from the complex and keep it removed. This is because the cpu_monitor utility will detect that the head has been removed and attempt to reenable it.

If it is desired to remove a head from the system complex by means of cpuconf, then the cpu_monitor utility must be disabled.

It should be further understood that the purpose of this utility is to monitor for downed heads and then return them to the complex.

If it's desired to keep the head out of the complex then this will have to be accomplished prior to boot with a powerdown, or removal from OS by means of xsys_config.

Al,

3.38.2 Saving Time on OS boot

Since the release of 10.0, there has been a mechanism in existence to save time when executing a disk preen on system reboots.

The mechanism basically tracks the accesses to individual file systems and marks it clean so that the disk will not have to been checked when the system is booted.

This is accomplished by the dirty bit in the superblock. When an access, or change has been made to this disk, the dirty bit is set. The dirty bit is cleared during a sync. A sync is executed by the update daemon every 30 seconds. So, when the disk is marked cleaned and therefore not preened on a reboot, this indicates that the disk has not been accessed in the past 30 seconds.

This mechanism is extremely reliable and should be trusted.

Al,

3.38.3 C3800 Bulkhead Cables

It should be understood that all C3800's ship with bulkhead cables attached to all CCU slots in the I/O bay. If no CCU is installed in a slot then differential cables are installed in the slot.

.....continued on next page.....

Differential devices include IDC's, ITC's, HiPPI's and TLI's.

It should never be necessary to install the cables after the system is installed, unless a single ended CCU (VIOP) is to be added to an existing configuration.

Al,

3.38.4 Running spu4000 Remotely

When running spu4000, on a C3800, in a remote situation, it is possible to display the test parameter's by way of the "par" command. This will display all of the system parameter's that can be displayed when running under the xdiag mode.

An example of the parameters can be seen in the example below:

```
test name: spu4000
cwd: /users/diaguser
cmdline: spu4000
****
STARTUP> par

- "CTI_path" "./"
- "CTI_pathname" "spu4000"
- "CUILexists" "0"
- "alarm" "5"
- "cleanup_messages" "0"
- "complete_on_fail" "0"
- "confirm_abort" "0"
- "cu_selected" "0"
- "current_description" ""
- "current_subtest" "0"
- "event_logger" "1"
- "fail_messages" "1"
- "failure_threshold" "10"
- "force_fail" "0"
- "ia_selected" "0,0,0,0,0,0,0,0,0,0"
- "init_messages" "0"
- "log_event" "0"
- "log_input" "0"
- "log_output" "0"
- "loop_count" "1"
- "looping" "0"
- "mb_selected" "0,0,0,0,0,0,0,0,0,0"
- "next_description" ""
```

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3.39.1 hpi4000 Diagnostic Failure on C3800

A problem has been identified in the "hpi4000" diagnostic when running on a C38 series system.

All diagnostic subtests will pass with the exception of subtest 2700. The following is an example of the error that will be seen:

```
     Subtest 2700   0:00:00   Microsecond Counter and Line Clock
                    0:00:01   failed

***** Mon Aug 17 14:06:34 1992 *****
Test:  hpi4000.t  1.4  Class: 2    Subtest: 2700 1.5 Count: 1    Error: 0
Failed: Microsecond Counter and Line Clock interrupt
---------- Trace point: 2700.1 ----------
Error 0x12: Line clock interrupt test
60 line clock interrupts occurred in one second
Minimum time between interrupts was 16657 uS
Maximum time between interrupts was 16667 uS
Splits array:
0x9ffd97 0xa03eb2 0xa07fcd 0xa0c0e8 0xa10202 0xa1431d 0xa18438 0xa1c549
0xa20663 0xa2477e 0xa28899 0xa2c9b3 0xa30ace 0xa34be9 0xa38d04 0xa3ce1e
0xa40f39 0xa4504a 0xa49165 0xa4d27f 0xa5139a 0xa554b5 0xa595cf 0xa5d6ea
0xa61805 0xa65920 0xa69a31 0xa6db4b 0xa71c66 0xa75d81 0xa79e9b 0xa7dfb6
0xa820d1 0xa861eb 0xa8a306 0xa8e421 0xa92532 0xa9664d 0xa9a767 0xa9e882
0xaa299d 0xaa6ab7 0xaaabd2 0xaaeced 0xab2e07 0xab6f22 0xabb033 0xabf14e
0xac3269 0xac7383 0xacb49e 0xacf5b9 0xad36d3 0xad77ee 0xadb909 0xadfa1a
0xae3b34 0xae7c4f 0xaebd6a 0xaefe85

Test 'hpi4000.t' failed
Elapsed time: 0:03:08
* * * * * Last command returned status 1 * * * * *
```

The reason, is the line clock is always read as 60hz in a c38 system. However, the diag. does not know this and calls a function that returns 50 in a 50hz country. Based on this wrong input, the diag will fail.

Please note that this diag. will pass on a C2.

-Kelvyn

3.39.2 Missing idcfmt Files

It has been discovered that "/usr/convex/idcfmt" and "/usr/lib/DB_idc" were left off V10.1.2, the idc driver does exist in the kernel.

It appears that this should have little effect on customers who upgrade, because older versions of "idcfmt" seem to work with 10.1.2. We have been using a 9.1 version of idcfmt with 10.1 on "mikey" for months. The problem appears on new loads of 10.1.2. So the only time this should effect our customers is when they have to load from scratch.

I waiting to find out what the resolution will be on distribution of the missing files.

Thanks, Chris

3.39.3 Version 3.1 C3800 Diagnostics

The 3800 diagnostic release 3.1 will soon be released. The following ia a list of enhancements and changes for this release.

Please, understand that ppc and bpc firmware is contained in this release, so allowances should be made for time to install. The firmware for each module will take approximately 3 1/2 minutes to download.

SST version 3.1 is a prerequisite for this release. Please ensure that SST is loaded first, or remove the old version before loading 3.1 Diagnostics.

POWER SYSTEM CHANGES:

1. Firmware

   BPC firmware is now at revision 3.17 - changes the default bay inlet and outlet temperatures:

   Inlet temps - warm=30 deg C and hot=35 deg C

   Outlet temps - warm=45 deg C and hot=50 deg C

   PPC firmware is now at revision 2.10: fixes primary power (300v) out-of-range problem. Caused message queue to fill up and hang the power system.

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2. Utilities

   altsetpts allows user to specify the bay inlet warm/hot temperatures and calculates the outlet warm/hot temperatures (+15 deg C). For example, altsetpts -t -w 32 -h 38 bay4 sets the inlet warm temp to 32 deg C and the inlet hot temp to 38 deg C.

   diaginit no longer displays the full bay status. Use -v option to get the full report.

   /diag/db/set_busses now sets the vtt on the MB board to -2.00V (was -1.95V).

   bpcwatchd has been modified to correctly handle "power off"unsolicited messages from the ppc. Now cleans up the Configuration Database to indicate the ppc is powered off.

   Software support for the new keyswitch.

UTILITY/TEST ENHANCEMENTS:

1. Utilities

   Added part numbers for RTIOP, new idc/itc board and rev C xbar backplane.

   Modified the SPU kernel to fix the window allocation problem (these are main memory windows).

   Added timestamps to cpualloc output for aid in determining down time.

   IA and SP soft errors are now stored in the Configuration Database and can be displayed using dump_soft_log.

   hard_logger now invokes the system_info script when processing APR errors. This includes the same data as when processing a "normal" hard error.

   Added call to the cleanup command in the initall script.

   Added the /etc/shells file to allow users to ftp into the SPU.

2. Diagnostics

   io5000 now supports the RTIOP board.

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Added additional short checking to the sp<->vp and ia8<->xbar tests in subtest 810 of spu4000.

Added source/sink signal bits to spu4000 subtest 810 error displays.

Added checking so cpu4333 can be run on a single head - cpucti deselects subtests that require 2 or more heads.

UTILITY/TEST FIXES:

1. Utilities

   cpualloc does not clear the cpu_os_req_? flag - allows head to come on-line on next reboot of ConvexOS.

   Errintd

   No longer attempts to log soft errors from a disabled head.

   Now disables APR when only a single head exists. APR is re-enabled when another head becomes available.

   Now correctly invokes the hard_logger when more than 2 heads pull a hard error.

   Fixed initialization of 8247 type SPs in sysreset to enable soft errors - no longer need to edit the /diag/db/scn_ovr file.

   Fixed the part number entry for the VIOP board - now accepts all assembly revs.

   Fixed ddb so displays tregs in the register display.

   Mminit

   Fixed intermittent sizing problem - will not need a 2nd run.

   Disallows downsizing of 256MB size boards to 128MB.

2. Tests

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Fixed timeout problems in cpucti when running cpu4331 in chain mode.

The SPU version of idcfmt now works, i.e. can format a disk.

Other fixes:

cpualloc.test now returns a 0 if no SST data patterns exists. Head will come on-line even if SST is never run.

The correct version of scan_trace is now installed - this is the 1X version.

Updated version of nts.

Can now specify parameters to mtst on command line:

mtst -d <addr> <byte_cnt> <xfr_type> <opcode> <even_pat> <odd_pat>

adb is now part of the diagnostic release.

CXTS SUPPORT: (CXTS will not be available in the field before December)

All error logging now uses RPC instead of system V IPC.

xsfp has a new boot option: cxts control boot.

xsfp starts 3 new daemons:

cxts_rt.prt
cxts_server.prt
cxts_ui

If CXTS daemons are not found, i.e. CXTS is not loaded, an error is printed in SPU Console window.

If CXTS daemons are found then startup of X environment after a SPU boot will take longer.

The "RPC: Program not registered" message during SPU boot can be ignored.

Any compiled user programs that log events need to be recompiled.

Al,

3.39.4 Version 3.1 SST

Version 3.1 of SST will soon be released. The primary reason for this release is for support of CXTS. In fact this is a prerequisite for 3.1 Diagnostics.

This is because the libraries are being converted from IPC (Internal Process Control) to RPC (Remote Process Control). If 3.0 SST is executed with 3.1 diagnostics then a hang will occur. If 3.1 SST is executed on 3.0 Diagnostics, the error messages "RPC:Program not registered" will occur during execution.

Al,

3.39.5 Running FDDI on a C3800

When running FDDI on a C3800 system, it is necessary to add the sticky bit to the file /mnt/os/drvfsd. This can be accomplished as follows:

chmod 4755 /mnt/os/drvfsd

This should be accomplished to prevent failures with vme based diagnostics and failures during boot of the type:

```
mminit: memory initialization complete
chguid: must be run as root or convexos.
drvfsd: warning: may need to be manually killed if kernel panics
[SPU @11:22:55] Errlog started: -l /mnt/errlog
[SPU @11:22:55] <Mon Sep 21 1992>
Loading vmunix
errintd(R1.0) started, options: -h -s
mm_sniff: sniff rate: 32.14 MB/day (15.86 days/pass)
vmunix: text: 1445888  data: 155648  tdata: 4096  tbss: 20480  bss: 1110016
```

After this the boot will abort. When this occurs, it is necessary to kill all drvfsd processes currently running on the SPU, except the most recent.

Al,

3.39.6 New Keyswitch for C3800

A new keyswitch will soon be available for the 3800 systems. It should be available to the field by the middle of November and will be in new builds in the first week of November.

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The part number for this keyswitch is 500-000542-200.

The prerequisite for this switch is 3.1 Diagnostics. The old keyswitch software will continue as default until the new switch is installed. Both versions of the software will be loaded as shown below:

xsfp.old_switch/xsfp.rc.old_switch

xsfp.new_switch/xsfp.rc.new_switch

When the new switch is installed, the new software can be initiated with the following script:

install_new_keyswitch

If necessary, the old switch software can be initiated by:

install_old_keyuswitch

The features of the new keyswitch is as follow:

1. Positions are Off-Remote-Local-Secure (was Off-Local-Secure-Remote).
2. xsfp now runs sys_shutdown in the Off position (was a hard bpc reset).
3. Key can be removed in the Off or Secure positions.
4. xsfp now waits 1 second after the last keyswitch interrupt before processing interrupt.

The procedure for installation of the new keyswitch is as follows:

1. Run sys_shutdown
2. Replace keyswitch
3. Run install_new_keyswitch
4. When prompted, reboot SPU

Al,

3.39.7 ConvexOs 10.1 and PETS

ConvexOS 10.1 will break all part1 tests in PETS. The mpa program was changed causing extra output to be logged in the answer files. A work around is to put the old mpa in PETS/bin and change the PETS/bin/path+aliases

```
from: set path = ($path /mnt/PETS/bin )
      rehash
      alias pets pushd /mnt/PETS

to:   set path = (/mnt/PETS/bin $path)
      rehash
      alias pets pushd /mnt/PETS
```

Ronnie Douthit

3.39.8 Unsupported Diagnostic Utilities

The following 3800 diagnostic utilities are no longer supported:

1) sys_con
2) xbinteg
3) xc_con
4) ncutestall

As many of you have already discovered, these utilities have many bugs and get worse with each release. All of the connectivity tests have been incorporated into spu4000 and ncutestall has been replaced with the diag cu4000.

The utilities will be removed from the 3.2 diagnostic release, to avoid confusion.

Al,

3.39.9 C3800 nvrf1 Failures with 10.2 ConvexOs Beta Release

It has been discovered that the vector clear solution, for the C3800 nvrf1 failures, was inadvertently left out of the 10.2 beta release that has been loaded up to this point. This is a minimal problem, as the nvrf1 is very intermittent and will not, now, crash the system, as APR will be functional on the systems with 10.2 installed.

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The production release of 10.2, due next week, will have the correction.

For all sites currently running 10.2, a patch will be generated.

Al,

3.39.10 xsysconfig Information

The memory size indicated in the xsysconfig display, on a C3800, is not valid until after the size utility of mminit has completed successfully.

Until mminit has completed successfully, on the individual memory board, the size indicated will generally be 512MB, but can be anything. When encountering failures with mminit, this is frequently mistaken for the problem, but this is not the case.

In addition, failures during mminit generally indicate a read, or write failure on the last physical memory board. This is quite often not the case and is far more frequently caused by another nmb, or other memory failure.

Al,

3.39.11 I/O Diagnostic Support for RTIOP

Diagnostic and cop data base support for RTIOP is included in I/O Diagnostic release 1.1, for 3200's. The diagnostic for RTIOP is included in io5000, but release 1.0 will fail subtest 101, with a RTIOP installed.

Although the RTIOP has 1MB of memory, as opposed to 512K for VIOP, the OS support for this does not exist. The diagnostic, however, does test it; and this is where the io5000 diagnostic in 1.0 will fail.

Al,

3.40.1 10.x OS ethernet failures

A problem has been identified with the VME Ethernet Controller that requires its firmware to be upgraded to v6.2. CCU Kernel aborts and system hangs have been experienced on customer systems during large file transfers across a network running 10.x OS.

Along with the firmware upgrade, it has been found that the VIOP must be at a Rev. K, or higher, and the VBCU must be at a Rev. L or higher.

An upgrade kit for the Ethernet firmware is available from logistics, and can be ordered using the 550-000151-250 part number. This kit will not be issued as an ECN, and should only be ordered on an as needed basis. This kit previously has been in the price book and cost $3000, but it is being removed from the price book and will be free, on demand.

-Kelvyn

3.40.2 IDC related ECC errors

It has been found that it is possible for the IDC to report an unrecoverable ECC error as a recoverable error. The problem is caused by the driver and can occur at any time.

What happens is that the IDC detects an ECC error on a sector and on the reread the failure persists. This is, so through the maximum number of retires which is 10. But even though the data was not recovered in the maximum number of retries, the error message "FSC 0x102c" is still used to represent the failure. As the data was not recovered, the recoverable ECC error is the improper designation.

To determine the recoverable errors from the unrecoverable errors, it is only necessary to examine the retry count. If the retry count is 10, or less, then the data was recoverable. If the retry count is equal to 11, then it is an unrecoverable ECC error and should be handled accordingly.

Al,

3.40.3 MIOP bug with io4000

A bug in io4000, previously corrected in past versions of diagnostics, has resurfaced in the 1.1 release of I/O diagnostics.

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The bug is a failure at subtest 200 when executed in dshell. A temporary solution is to execute the .t version directly out of /mnt/test.

Wesley Mathies

3.40.4 8mm Tape firmware failures

The following problem has been discovered with the 8mm tape drive firmware.

The problem is characterized by one or more drives "hanging" with the select and ready lights on. The hangs cannot be corrected without cycling the power on the drive(s). No errors are logged to the error log. Jobs using the drives may or may not run for awhile before the hangs occur. The hangs occur even when the drives are controlled OFF by tpconfig. If the drives are controlled ON, it may cause problems (hang or termination) with the tpdaemon.

The hangs are due to old revisions of the 8mm drive firmware. Replacement of the old PROMS with the most current ones corrects the problem.

The old firmware levels are:	MXPROM	SVPROM
	4$24	B018
	425A	B019
The latest firmware levels are:	MXPROM	SVPROM
	2640	C034

Terri Thomas

3.40.5 C3800 APR Failures

There have been some isolated instances of APR failing to clear a hard error on a C3800 and prevent the system from crashing. There are two variations of the problem and are detailed as follows:

1) The first failure is a system hang during execution of the hard logger. There is no other indication, but it cannot be cleared, except by reboot.

.....continued on next page.....

2) The second variation is that the hard error cannot be cleared and the system crashes and executes an osclean. An example is below:

```
HardLog End (DiagER483): Hard_logger completion

 ****
ERRINTD: Checking if OS has cleaned up CPU
ERRINTD: Re-enabling local enables
ERRINTD: Awaiting the cleanup of a DEAD CPU
Unable to clear hard error on CPU 1 - calling OSCLEAN.
```

It should be understood that the instances of these problems have been rare and is not understood. It is possible that the failures are due to the hard error, or some other hardware failure, but until more information is collected this is a mystery.

In order to perform initial analysis of the failures, it is requested that the following script be loaded on each SPU and executed directly following one of these events.

```
#!/diag/bin/dsh
#script to dump lower 4k of memory.
#
   cleanup
   cleanup
   cleanup

   filext=`date +%m%d%y%H%M`
   cd /mnt/os
   fprint "0,0x200/l\n\$q\n" | jpd -n 2>&1 > /sst/apr.out.$filext
   echo "" >> /sst/apr.out.$filext

#
# Grab the vmunix file that is in /mnt/os and tar that together with
# the apr file. So that we have a single file to get.
#

   tar -cf /sst/apr.out.${filext}.tar vmunix -C /sst apr.out.$filext
   cd /sst
   compress apr.out.${filext}.tar
   exit 0
```

The purpose of this script is to dump the first page of memory and save the contents of the pc. This is all appended to the vmunix, compressed and saved in a file. This file should then be forwarded to the TAC for analysis.

Al,

3.40.6 New C3800 Diag Release

In a previous tech bulletin, the enhancements and fixes in 3.1 diags were listed. This release has since been replaced with version 3.2. This presents no problems except for the designation change.

Al,

3.41.1 C3800 APR Information

As was reported last week, there have been occurrences of APR not being able to clean up after a head crash and ultimately result in a system crash. A script was sent to the field to evaluate these failures. Initial analysis indicates that some portion of these crashes are due to failures within the kernel.

As reported previously, APR cannot recover from a crash in the kernel. This crash should generate a "FATAL CONVEX UNIX ERROR". In fact this happens, but in many instances, due to a defect in errintd, the Fatal error does not appear in the errlog, or is only partially seen. It does, however, show up on the CONVEX_OS Screen.

This can be confirmed with a register dump of the head. The pc value should indicate that it was in the kernel.

As the final evaluation is not complete, it is important that the script still be executed after crashes of this nature.

Al,

3.41.2 MCM3 DMM Identification

The current dmm's shipped, for MCM3's, have a 411-000204-500 number etched on the dmm itself. This number should not be confused with 204-200 number used for the 2MB dmm's. The 500 level number indicates that it is a fab level.

To distinguish between the 1204 and 204 dmm's it is necessary to examine the number on the dram's themselves. If the dram has a 4400 within the dram part number, then the dram is a 4MB chip and is used on the 1204 dmm. If the part number for dram has a 256 in it, then the chip is a 1MB dram and is used on the 204 dmm. This will work for all chip manufacturer's numbers.

In the past an orange, or yellow sticker was placed on the dmm to identify it, but this practice has been discontinued.

For more information on the MCM3 and dmm's, please review the past tech bulletins on this subject.

Al,

3.41.3 ConvexOs 10.2 nvrf1 patch

We currently have a patch that addresses the return of the nvrf1 failures with 10.2 OS.

The patch is 10.2.141. This patch will only be used with the current Beta release of 10.2, as the patch will be included in the production release.

At current, the production release of 10.2 is not scheduled to finish qual before the end of October. This schedule will only be met if no major problems are discovered.

At this time, the beat release of 10.2 with all available patches, is equivalent to the production release.

The current patches available, for 10.2 are as follow:

10.2.128	SCSI driver
10.2.129	VME Async printer
10.2.131	crashes caused by stripe driver
10.2.132	Tape driver
10.2.133	Stripe hangs
10.2.134	crashdump
10.2.135	Customer Specific Patch
10.2.137	Ethernet Driver
10.2.138	PTE Violations
10.2.139	Tape System
10.2.140	Stripe driver related hangs
10.2.141	NVRF1 Patch
10.2.142	New cpu_monitor for APR

Of course, 10.2 OS for specifically for 3800's and should not be used on any other system.

Al,

3.42.1 1.5gb RDS Disk Support

The 1.5 GB rds disk has been released The prereq's are:

1) 10.1 OS for total support. 10.0 OS has the driver and needs the disktab entry. The disktab entry appears below:
2) 1.1 I/O Diags (or entries in dskfmt file)
3) ESDI controller p/n 220-000025-200 (See Tech Bulletin 3.35.14)

```
dkd-287|DKD-287|dkd287:\
        :ty=winchester:se#512:ns#80:nt#5:nc#6300:rm#3600\
        :pa#125952:ba#8192:fa#1024:\
        :pb#503936:bb#8192:fb#1024:\
        :pc#2505600:bc#65536:fc#8192:\
        :pd#125952:bd#8192:fd#1024:\
        :pe#755968:be#4096:fe#512:\
        :pf#251904:bf#4096:ff#1024:\
        :pg#1133952:bg#4096:fg#512:\
        :ph#741504:bh#4096:fh#1024:
```

The ioconfig entry is as follows:

```
vme 0
  ctrl DKC-203 csr 0xc00 int 3
    unit 0 type DKD-287
```

As mentioned above, it is possible to add the entry in the DB_diskfmt file to gain diagnostic and format capabilities. An example of the entry is shown below:

```
# DB_diskfmt - file of disk parameters
#
# >>>> WARNING - DO NOT USE 'diskfmt' TO FORMAT! It is no longer compatible
# >>>>           with the CONVEX FORMAT! Instead, format MBUS-attached drives
# >>>>           with 'dev4110' and VME-attached drives with 'dev4120'. Note
# >>>>           that the DKD-008 and any future SMD drives that are attached
# >>>>           to a Xylogics 450 or 451 controller will be specified as
# >>>>           having one less than the actual number of cylinders. This
# >>>>           prevents erasure of the defect cylinder if 'diskfmt' is
# >>>>           accidentally used to reformat a drive. DKD-001, DKD-002,
```

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```
# >>>>          DKD-005 on the Xylogics 450 or 451 controller and all
# >>>>          drives used on other controllers will have the actual number
# >>>>          of cylinders as specified below.
#
# KEY FOR DRIVE NAMES (unformatted capacity is given in parentheses):
# Name          Description                 Name          Description
# DKD-001       Fujitsu Eagle (452MB)       DKD-008,208   NEC 2363 (1080MB)
# DKD-002       CDC 9766 (300MB)            DKD-214       Hitachi DK514-38 (356MB)
# DKD-005,206   NEC 2352 (500MB)            DKD-280       Fujitsu 2382K (1GB)
# DKD-281       CDC 9720 (1GB)              DKD-282       Fujitsu 2372 (800MB)
# DKD-283       CDC 9720-850 (851MB)        DKD-287       Micropolis ESDI (1.53GB)
# DKD-284       Hitachi DK515-78 (780MB)
#
#------- INTERPHASE 4201 ESDI CONTROLLER (VME) --------
#    a      b    c    d  e  f    g     h     i  j  k  l  m  n  o  p
DKD-214  0  903  14 51 50 4736 30240 5  5 1  8  8 esdi 2-7 n
DKD-284  0 1361 14 69 68 4744 40960 9  7 1  8  8 esdi 2-7 n
DKD-287  0 2100 15 81 80 4776 48608 7 11 1 12 12 esdi 1-7 n
#
# LEGEND:
# a - drive name                Must be DKD-0XX for Multibus and DKD-2XX for
#                               VMEbus
# b - disk type                 For Xylogics controller
# c - # of cylinders            DKD-008 and future drives on Xylogics 451
#                               will
#                               have one less than the actual number.
# d - # of heads
# e - # of physical sectors     Number of actual sectors excluding runt
# f - # of logical sectors      Number of physical sectors minus number of
#                               spares
# g - bits per sector           Number of bits between sector pulses
# h - bytes per track           Total number of unformatted bytes per track
# i - skew                      Sector offset from one head to the next
#                               Must be 1 when using Xylogics 450/451 cntlr
# j - # of relocation tracks    .5% of number of cylinders. Raise fractional
#                               part to next higher whole number.
#                               Ignored by dev4110 (Multibus formatter)
# k - interleave                sector separation between consecutive sectors
#                               Currently must be 1 for Xylogics 450/451
#                               cntlr
```

.....continued on next page.....

# l - gap 1 size	Number of halfwords in gap before header
#	(2 bytes per halfword)
#	Ignored by dev4110 (Multibus formatter)
# m - gap 2 size	Number of halfwords in gap following header
#	(2 bytes per halfword)
#	Ignored by dev4110 (Multibus formatter)
# n - drive interface	Used to determine how to read manufacturer's
#	defect map. Currently, smd or esdi
#	Ignored by dev4110 (Multibus formatter)
# o - data encoding scheme	Way data is encoded on the media. Used to
#	select patterns for pattern test.
#	Currently mfm, 2-7 or 1-7
# p - Are spares interleaved	For Xylogics, 'y'. For Interphase, 'n'.

Al,

3.42.2 C3800 cpu_config Setup

It is recommended that the FAILURE_COUNT entry in /etc/cpu_monitor.config be modified to a value of 2. The default parameter is set to 4 this will allow five (5) crashes on the same head in a 24 hour period.

As the job that is executing on the specific head will abort, this many failures can create difficulties for a customer trying to complete a specific job.

Al,

3.42.3 New MCM3 Information

It should be understood that the 3230 MCM3 has replaced the 1230 and 2230 MCM3's in new and upgrade shipments. This can cause problems in attempting to upgrade memory on systems running lower revision diagnostic levels.

The 3230 was not entered in the DB_cop file until the release of 5.0 Diags. But, the MCM3 appeared in the 4.1 release.

The 3230 is functionally equivalent to the previous boards and require no modifications not contained in the initial release. Therefore, it is perfectly acceptable to enter the 3230 part number in the DB_cop file, without having to upgrade diagnostics.
Al,

3.42.4 C3800 Hard Error ucode_pulled_hard_err

The C3800 hard error "ucode_pulled_hard_err" has been showing up more often of late. This failure is not a traditional hard error and is more closely related to the "Fatal CONVEX UNIX ERROR". In fact the error is almost identical in content to the ASP104 seen on the C2 class systems. In other words, this failure can be caused by almost anything.

When encountering this error, it's best to collect as much information as possible. This will, especially, include a dump of xbar_err. This is because the xrt's can stop during this failure and generate some unintelligible information.

One other piece of information displayed by the extractor is the uirl_upc, which is the microsequencer pc. This is equivalent to the ipc on the C2. The legitimate codes are bf4, bf6, bf8, bfa and bff, where:

```
bf4 = invalid fault vector
bf6 = rtnc frame w/FRL nonzero
bf8 = System resource structure underflow
bfa = pulled by diag instruction
bff = recursive page fault
```

NOTE These are identical to C2 error codes.

An example is shown below:

```
Hard error Summary

------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    0            SP_TYPE               1
sp_npsw.ucode_pulled_hard_err
==================================================================
spl:npsw.ucode_pulled_hard_err = 1
The microusequencer detected an unhealthy situation and asserted
a hard error to indicate this.
uirl_upc = bf8 **** System Resource Structure (SRS) Underflow
==================================================================
+++>
<Thu Oct 8 08:27:57 1992>   logmsg:../logmsg.c:56
Hard Error (DiagER349):logmsg: General purpose event
Source: sp_npsw_ucode_pulled_hard_err
@extractor=sp_npsw_ucode_pulled_hard_err @board_type=sp @port=1
****
```

Al,

3.42.5 C3800 wredc_par_err

It should not be taken for granted that "wredc_par_err" involves only the nmb. The accompanying hard errors should always be examined to determine if another source of the failure may exist. This advice should be followed for any traditional memory error. Although the error's can appear, at first glance, to be obvious, this is not necessarily true. It should be understood that extractors will execute in a predictable order and always in that order. This fact can further complicate matters.

Any hard error sequence from the hard_logger should, initially, be evaluated for the proper architectural sequence of the errors. If this is not accomplished then the wrong solution will be applied to the failure.

In the harderror sequence below, the failure is actually caused by an NSP. This relationship can be seen in both harderror#1 and #2. Further evidence can usually be obtained from examining the crossbar for errors. A hint might be the existence of a iso, or ise parity error. Due to the location of the input staging register, it can suggest that the failure can be found external to the memory board.

The second hard error sequence shows a double bit rdedc error. But, because of the presence of the "iso_addr_par_err", the XS0O should be suspected.

Further evaluation should always occur when unsure of the source.

EXAMPLE 1

```
Hard error Summary
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE    EXTRACTOR
-----------     ----------          ---------    ---------
    0            MB_TYPE               0         mb_odd_bank_wredc_par_err
===================================================================
 ODD side 'bank_wredc_perr': PARITY error detected in MB0
-------------------------------------------------------------------
 WREDC PARITY error detected by BCGA 0 in bank 0 ( => BANK_0o)
 during a NOP.
     -----  --------------------------------
       1       mbs0:bc[0].sys.bct10_merr_pe
       1       mbs0:nmc0o_rerr
       1       mbs0:nmc0o_rla_ecc_check1
      43b00       mbs0:nmc0o_data
          f       mbs0:nmc0o_ecc (parity)
          0       mbs0:bc[0].bcga_log.bct10_cycle
        600       mbs0:bc0_bank0_log_addr (phys_addr is 3000)
-------------------------------------------------------------------
```

.....continued on next page.....

```
+++>
<Thu Oct 8 04:57:46 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_odd_bank_wredc_par_err
@extractor=mb_odd_bank_wredc_par_err @board_type=mb @port=0
****

-------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    1            MB_TYPE               0          mb_iso_data_perr
===================================================================
 ODD side 'iso_data' ctl_par_err detected in discrete input staging
 registers by MB0. Request came from SP1 through the XS<odd>.
-------------------------------------------------------------------
PARITY CHECK - The XBAR data is saved in lookaside registers in
               the XS1 and XS0. This is the data that the XBAR
               sent to the NMB for this request. Any difference
               between the XBAR data and the NMB data may indicate
               a connectivity problem between the XBAR and the NMB.
               Otherwise the XBAR or the SP-XBAR connection is bad.
-------------------------------------------------------------------
          Data                  Scan Field
      ----------------------------------------
        ***Data was not preserved in SP1***
      ----------------------------------------
      00  04  3b  00    xslo:wr_data_lsd2[0]<31..0>
       1   1*  1*  1    xslo:wr_par_lsd2[0]<0..3>
      ----------------------------------------
      00  04  3b  00    mbs0:iso_sys.rwro_data<31..0>
       1   1*  1*  1    mbs0:iso_sys.rwro_par<0..3>
      ----------------------------------------
      * indicates parity error.
 Note that quantities in "<>" delimiters are bit descriptors.
 They are not part of the scan field name.
-------------------------------------------------------------------
+++>
<Thu Oct 8 04:57:47 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_iso_data_perr
@extractor=mb_iso_data_perr @board_type=mb @port=0
****
```

.....continued on next page.....

```
-------------------------------------------------------------------
HARDERROR #    BOARD TYPE          PORT/SIDE    EXTRACTOR
-----------    ----------          ---------    ---------
    2           XS1_TYPE              1          xs1.send_par_err_mb0
===================================================================
 Send parity error detected by MB0 from SP1 in XS0/10
          Data                  Scan Field
     ----------------------------------------
       ***Data was not preserved in SP1***
     ----------------------------------------
     00  04  3b  00    xs1o:wr_data_lsd2[0]<31..0>
      1   1*  1*  1    xs1o:wr_par_lsd2[0]<0..3>
     ----------------------------------------
     00  04  3b  00    mbs0:iso_sys.rwro_data<31..0>
      1   1*  1*  1    mbs0:iso_sys.rwro_par<0..3>
     ----------------------------------------
     * indicates parity error
-------------------------------------------------------------------
 xs1o:m_err_en<0> = 1
 xs1o:send_par_err<0> = 1
+++>
<Thu Oct 8 04:57:49 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: xs1_send_par_err_mb0 @extractor=xs1_send_par_err_mb0
@board_type=xs1 @port=1
****

+++>
<Thu Oct 8 04:57:49 1992>      /diag/bin/hard_logger.exc:../hard.c:187
HardLog End (DiagER483): Hard_logger completion
```

EXAMPLE 2

```
Hard error Summary

-------------------------------------------------------------------
HARDERROR #    BOARD TYPE          PORT/SIDE    EXTRACTOR
-----------    ----------          ---------    ---------
    0           MB_TYPE               4          mb_odd_bank_rdedc_multi_bit_err
===================================================================
 ODD side 'bank_rdedc_multi_bit_err' detected in RDEDC of MB4.
-------------------------------------------------------------------
 MULTI-BIT error in BCGA1 BAN1 ( => BAN_5o) detected by
 RDEDC during READ operation.
-------------------------------------------------------------------
```

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```
          ODD side BCGA error log:
     -----  -------------------------------
       1      mbs4:bc[1].sys.bctl1_rtn_merr
          1      mbs4:bc[1].bcga_log.bctl1_cycle
     e2d7b5      mbs4:bc1_bank1_log_addr (phys_addr is 716bda8)
     -----  -------------------------------
          ODD side RDEDC error log:
     -----  -------------------------------
   17fefb80      mbs4:rdedc.log[1].error_data
         de      mbs4:rdedc.log[1].error_ecc
         ad      mbs4:rdedc.log[1].error_cmp
-----------------------------------------------------------------
<Tue Oct 6 11:47:03 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_odd_bank_rdedc_multi_bit_err
@extractor=mb_odd_bank_rdedc_multi_bit_err @board_type=mb @port=4
****
-----------------------------------------------------------------
HARDERROR #    BOARD TYPE         PORT/SIDE    EXTRACTOR
-----------    ----------         ---------    ---------
    1           MB_TYPE              4          mb_odd_bank_ctl_err
=================================================================
 ODD side 'bank_ctl_err': Request to busy bank detected in MB4.
-----------------------------------------------------------------
  Request while bank busy error detected by BCGA 3 in bank 3
  ( => BAN_fo). No other error state saved for this bank.
     -----  -------------------------------
       1      mbs4:bc[3].sys.bctl3_ctl_he
-----------------------------------------------------------------
+++>
<Tue Oct 6 11:47:04 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_odd_bank_ctl_err
@extractor=mb_odd_bank_ctl_err @board_type=mb @port=4
****
-----------------------------------------------------------------
HARDERROR #    BOARD TYPE         PORT/SIDE    EXTRACTOR
-----------    ----------         ---------    ---------
    2           MB_TYPE              4          mb_iso_addr_perr
=================================================================
 ODD side 'iso_addr' ctl_par_err detected in discrete input staging
 registers by MB4. Request came from SP4 through the XS<odd>.
-----------------------------------------------------------------
```

.....continued on next page.....

```
  PARITY CHECK - The XBAR data is saved in lookaside registers in
                 the XS1 and XS0. This is the data that the XBAR
                 sent to the NMB for this request. Any difference
                 between the XBAR data and the NMB data may indicate
                 a connectivity problem between the XBAR and the NMB.
                 Otherwise the XBAR or the SP-XBAR connection is bad.
-------------------------------------------------------------------
 Scan fields:  NMB                        XBAR
     ----------------------------      ----------------------------
     1c mbs4:iso_sys.addr               1c xs0o:addr_lsd2[4]<28..22>
      0 mbs4:mbo_ctl_par<0>              0 xs1o:ctl_par_lsd2[4]
                                         0 xs0o:send_par_err<4>
-------------------------------------------------------------------
 Note that the <28..22> notation is not part of the scan field
 name, but represents which bits of the bus are being displayed.
 Bit mapping is relative to the schematic. Addr<28> from the
 schematic corresponds to addr<25> in the actual scan field data.
-------------------------------------------------------------------
  SANITY CHECK - Each BCGA in the table below should contain the
                 same data as the discrete registers above. Data
                 mismatch indicates a failure on the NMB. Slow
                 (bad) timing should affect the BCGAs first.
-------------------------------------------------------------------
 Scan fields:  NMB                Location:    BCGA
     ----------------------------             ----------------------
     1c mbs4:bc0_sys_addr<28..22>              0
      0 mbs4:bc[0].sys.ris_ctl_par_3_0<0>
     1c mbs4:bc1_sys_addr<28..22>              1
      0 mbs4:bc[1].sys.ris_ctl_par_3_0<0>
     1c mbs4:bc2_sys_addr<28..22>              2
      0 mbs4:bc[2].sys.ris_ctl_par_3_0<0>
     1c mbs4:bc3_sys_addr<28..22>              3
      0 mbs4:bc[3].sys.ris_ctl_par_3_0<0>
-------------------------------------------------------------------
     * indicates parity error.
-------------------------------------------------------------------
<Tue Oct 6 11:47:06 1992>    logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_iso_addr_perr
@extractor=mb_iso_addr_perr @board_type=mb @port=4
****
```

.....continued on next page.....

```
-------------------------------------------------------------------
HARDERROR #     BOARD TYPE          PORT/SIDE     EXTRACTOR
-----------     ----------          ---------     ---------
    3             MB_TYPE               4          mb_even_bank_ctl_err
===================================================================
 EVEN side 'bank_ctl_err': Request to busy bank detected in MB4.
-------------------------------------------------------------------
  Request while bank busy error detected by BCGA 7 in bank 3
  ( => BAN_fe). No other error state saved for this bank.
     -----  --------------------------------
       1       mbs4:bc[7].sys.bctl3_ctl_he
-------------------------------------------------------------------
<Tue Oct 6 11:47:07 1992>     logmsg:../logmsg.c:56
Hard Error (DiagER349): logmsg: General purpose event
Source: mb_even_bank_ctl_err
@extractor=mb_even_bank_ctl_err @board_type=mb @port=4
HardLog End (DiagER483): Hard_logger completion
```

Al,

3.42.6 VIOP Memory Pages With Ethernet

The VIOP memory page allocation list is incorrect for ethernet when loading the ethernet related patches 10.0.146, 10.1.138 and 10.2.137. These patches include a new ethernet driver which uses 17 pages instead of the 11 pages that are consumed with the old driver.

In addition, this new ethernet driver is not tunable. As this driver only executes a single process instead of the four used by the previous driver, any effort to detune will result in a major loss of performance.

The past procedures for detuning the ethernet is now invalid.

This change in memory usage is the reason that VME configurations are running out of VIOP memory.

Al,

3.42.7 C3800 APR Functionality Test

In order to test APR functionality it is only necessary to remove the head from the OS by cpuconf -d <head no.> and wait for APR to execute sst and return the head on line. If this does not occur in less than 6 minutes then something is configured wrong with the cpu_monitor, or the spu level support files.

This will work because the cpu_monitor daemon is not part of the hard_logger mechanism and only monitors head availability. When the head is removed from the configuration, cpu_monitor will execute sst on the removed head and restore it to the configuration.

Al,

3.42.8 C3400 System Spares Matrix

C3400 SERIES BOARD SET

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
410-002223-200	SP5	x	x	x
410-003224-200	PI2	x	x	x
410-001235-200	CUJ, Note 1	x	x	x
410-002235-200	CUJ Note 2	x	x	x
410-002236-200	JCPU	x	x	
410-003236-200	JCPU	x	x	
410-004236-200	JCPU			x
410-005236-200	JCPU			x
410-003180-200	JSM System Monitor	x	x	
411-001340-200	SM2 System Monitor	Note 3	Note 3	x
410-002230-200	MCM3 without DMM's	x	x	x
411-000204-200	2mb DMM	x	x	x
411-001204-200	8mb DMM	x	x	x

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C3400 SERIES CABINET PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
411-002222-200	Fan Fail Sense board	x	x	
411-001339-200	Fan/environmental Sense			x
207-000009-201	Cartridge tape drive, 150mb	x	x	x
500-000250-200	Temperature probe assembly, inlet air	x	x	x
500-000251-200	Temperature probe assembly exhaust air	x	x	x
411-001221-200	Fan AC power distribution board	x	x	
604-080001-200	Delay line cable assembly		x	
604-160001-200	Clock line cable assembly		x	
411-000158-200	SPU disk paddle board assembly	x	x	x
411-000276-200	MEM_TOP Term Card	Note 4	Note 4	Note 5
411-000277-200	MEM_BOT Term Card	Note 4	Note 4	Note 5
411-000278-200	PI2_TOP Term Card	x	x	x
411-000279-200	PI2_BOT Term Card	x	x	x
411-001354-200	C3400-EX CPU Terminator Card			Note 6
204-000022-200	SPU disk, 477mb	x	x	x
500-000347-200	Blower Assy, Fn-2, Fn-4	Note 7	x	
500-000348-200	Blower Assy, Fn-1, Fn-3, Fn-5, Fn-6		x	
500-000383-200	Blower Assy, I/O and Memory areas			x
500-000384-200	Blower Assy, CPU Areas			x
500-000355-200	Blower sensor			x

C3400 SERIES POWER SYSTEM PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
500-000338-290	Power supply, -2vdc, 800w	x	x	
500-000338-291	Power supply, -4.5, 1800w	x	x	
500-000338-292	Power supply, +5vdc, 2000w	x	x	
500-000339-290	Power supply, multivolt 1000w	x	x	
500-000339-295	Power supply, multivolt	x		
500-000369-200	Power Controller - Domestic		x	
500-000367-200	Power controller - International		x	
500-000381-290	Power controller - Universal	x		
500-000218-200	Indicator panel - Domestic			
500-000218-202	Indicator panel - International			x
500-000415-201	Power controller - Universal			x

.....continued on next page.....

C3400 SERIES POWER SYSTEM PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	Used In C3400	Used In C3400-EX
500-000438-200	Power supply, -2v 800w			x
500-000438-201	Power supply, -4.5v 1800w			x
500-000438-202	Power supply, +5v, 2000w			x
500-000439-200	Power supply, multivolt, 1000w			x
500-000533-200	Transformer, blower step-up, 60hz			x
500-003131-200	Processor control panel assembly			x

Note 1: Required for Realtime systems

Note 2: Standard C3400 systems only. No support for Realtime systems

Note 3: Can be used in C3400-ES and C3400 with appropriate firmware.

Note 4: C3400 and C3400-ES use assembly revision A.0

Note 5: C3400-EX uses assembly revision B.0

Note 6: This terminator is required on a C3400-EX in any slot that does not have a matching CPU board installed. E.G. if a CPU board is installed in CPU-4 and no CPU is installed in CPU-5, a terminator card must be installed in the CPU-5 slot.

Note 7: Used for all fan locations in C3400-ES

* Dave Muir *

3.42.9 Javelin Diagnostic/Database tape V1.4.

Release of V1.4 of the C3400 Diagnostic/Database tape has microcode Version 5.28. This microcode corrects several conditions in the microcode that can cause system hangs, file system corruption, and several types of 1122 hard errors.

It is important to install this version of the Diag/database tape in all versions of the C3400 systems as soon as possible.

* Dave Muir *

3.42.10 C3800 SPU Backup and Restore

Backup

The "/etc/backup" script looks at "/etc/fstab" to determine which file systems to dump.

Here is what "fstab" looks like on a SPU running SpuOS 2.0 and Diags 3.0.

/dev/sd0a / 4.2 rw 1 1
/dev/sd0f /diag 4.2 rw 1 3
/dev/sd0e /mnt 4.2 rw 1 4
/dev/sd0h /sst 4.2 rw 1 5
/dev/sd0g /usr 4.2 rw 1 2

"/etc/backup" will dump the file systems in the following order:
/
/diag
/mnt
/sst
/usr

Be sure to make note of the order the file systems are dumped, so you will have the proper info if you need to "restore" from the "backup" tape.

To backup the SPU do the following:

Insert a write enabled tape in the DAT drive.

spu> su to become root.
spu\> cd /
spu\> /etc/backup

This will dump all of the SPU file systems onto one tape.

Restore

Restoring "/"

At the ">b" prompt
Insert the "SpuOS" tape in the DAT drive.

.....continued on next page.....

```
>b b st()
Probing Memory.....
Booting from: st(0,0,0)

What would you like to do?
1 - install mini-root
2 - exit into single user shell
Enter a 1 or 2: 1
.
Do you want to format and/or label disk "sd0"?
1 - yes, run format
2 - no, continue loading miniroot
3 - no, exit into single user shell
Enter a 1, 2, or 3: 2
.
Problem with tape: what do you want to do?
1 - retry the tape "st0"
2 - use a different tape unit
3 - abandon miniroot install and enter single user shell
Enter a 1, 2, or 3: 1
.
Mini-root installation complete.
.
What would you like to do?
1 - reboot using just-installed miniroot
2 - exit into single user shell
Enter a 1 or 2: 1 .
.
You will see boot messages and then the miniroot prompt "#".
.
# newfs /dev/rsd0a
# mount /dev/sd0a /a
# cd /a
Insert the "backup" tape in the DAT drive.
# mt -f /dev/rst0 rew
# restore xf /dev/rst0
.
.
Specify next volume#: 1
```

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```
# Set directory mode, owner, and times.
set owner/mode for ".”? [yn] y
# cd /
# umount /a
#/etc/fsck /dev/rsd0a
# cd /usr/kvm/mdec
# installboot /boot bootsd /dev/rsd0a
# /etc/reboot
```

Restoring "/usr"

At the ">b" prompt
Insert the "SpuOS" tape in the DAT drive.

```
>b b st()
Probing Memory.....
Booting from: st(0,0,0)

What would you like to do?
1 - install mini-root"
2 - exit into single user shell"
Enter a 1 or 2: 1
.
.
Do you want to format and/or label disk "sd0"?
1 - yes, run format
2 - no, continue loading miniroot
3 - no, exit into single user shell
Enter a 1, 2, or 3: 2
.
.
Problem with tape: what do you want to do?
1 - retry the tape "st0"
2 - use a different tape unit
3 - abandon miniroot install and enter single user shell
Enter a 1, 2, or 3: 1
.
.
Mini-root installation complete.
```

.....continue on next page....

What would you like to do?
1 - reboot using just-installed miniroot
2 - exit into single user shell
Enter a 1 or 2: 1
.
.
You will see boot messages and then the miniroot prompt "#".
.
newfs /dev/rsd0g
mount /dev/sd0a /a
mount /dev/sd0g /a/usr
cd /a/usr

Insert the "backup" tape in the DAT drive.

mt -f /dev/rst0 rew
restore xfs /dev/rst0 5
.
.
Specify next volume#: 1
Set directory mode, owner, and times.
set owner/mode for ".'? [yn] y
cd /
umount /a/usr
umount /a
/etc/fsck /dev/rsd0g
/etc/reboot

Restoring "/diag"

Boot the system to single user.

>b b -s
/etc/newfs /dev/rsd0f
mount /dev/sd0f /diag
cd /diag

Insert the "backup" tape in the DAT drive.

mt -f /dev/rst0 rew

.....continue on next page.....

```
# restore xfs /dev/rst0 2
.
.
Specify next volume#: 1
set owner/mode for ".”? [yn] y
# cd /
# umount /diag
# /etc/fsck /dev/rsd0f
# ^d (Go to multi-user)
```

Restoring "/mnt"

Boot the system to single user.

```
>b b -s
# /etc/newfs /dev/rsd0e
# mount /dev/sd0e /mnt
# cd /mnt
```

Insert the "backup" tape in the DAT drive.

```
# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 3
.
.
Specify next volume#: 1
set owner/mode for ".”? [yn] y
# cd /
# umount /mnt
# /etc/fsck /dev/rsd0e
# ^d (Go to multi-user)
```

Restoring "/sst"

Boot the system to single user.

```
>b b -s
# /etc/newfs /dev/rsd0h
# mount /dev/sd0h /sst
```

.....continued on next page.....

```
# cd /sst
Insert the "backup" tape in the DAT drive.

# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 4
.
Specify next volume#: 1
set owner/mode for ".'? [yn] y
# cd /
# umount /sst
# /etc/fsck /dev/rsd0h
# ^d (Go to multi-user)
```

Dan Brenner

3.43.1 3800 XSFP Key-Switch Positions and Power-up Actions

1 Key Off

1.1 SPU and 3800 powered down. Power-up Boot Mode doesn't matter. When the SPU boots, it will start the window manager and open the SPU CONSOLE, Xterm, XSFP and the Icons windows. It will open the CONVEXOS CONSOLE window and then iconify it. The SPU will then wait for further instructions.

1.2 SPU and 3800 powered up and then key to off. With old style keyswitch, will force 3800 power system into reset and immediately power down the 3800. With new style switch, will call "sys_shutdown" utility and do a controlled power down of the 3800.

2 Key Local

2.1 When the key is in the local position and the SPU is booted, the Xwindow pointer may be moved to any position on the screen. The user "rmtdiag" is not allowed to login.

2.2 SPU and 3800 powered down. Power-up Boot Mode in "diagnostics". When the SPU boots, it will start the window manager and open the SPU CONSOLE, Xterm, XSFP, CONVEXOS CONSOLE and the Icons windows. The SPU then waits for further instructions.

2.3 SPU and 3800 powered down. Power-up Boot Mode in "normal OS". When the SPU boots, it will start the window manager and open the SPU CONSOLE, Xterm, XSFP, CONVEXOS CONSOLE and the Icons windows. The SPU will then execute "diaginit" which will power-up the 3800. After the "diaginit" is complete, the SPU will execute a "boot multi" command and boot the 3800.

2.4 SPU and 3800 powered down. Power-up Boot Mode in "alternate OS" When the SPU boots, it will start the window manager and open the SPU CONSOLE, Xterm, XSFP, CONVEXOS CONSOLE and the Icons windows. The SPU will then execute "diaginit" which will power-up the 3800. The SPU then waits for further instructions.

3 Key Remote

3.1 When the key is in the remote position and the SPU is booted, the Xwindow pointer may be moved to any position on the screen. The user "rmtdiag" is allowed to log in.

3.2 SPU and 3800 powered down. Power-up Boot Mode in "diagnostics". Functions the same as when key is in local.

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3.3 SPU and 3800 powered down. Power-up Boot Mode in "normal OS". Functions the same as when key is in local.
3.4 SPU and 3800 powered down. Power-up Boot Mode in "alternate OS" Functions the same as when key is in local.

4 Key Secure

4.1 When the key is in the secure position and the SPU is booted, The Xwindow pointer is locked into the CONVEXOS CONSOLE window. The ^p and ^d functions are disabled. The modem's "getty" is killed and the ethernet is shutdown.

4.2 SPU and 3800 powered down. Power-up Boot Mode in "diagnostics". Functions the same as when key is in local. 4.3 SPU and 3800 powered down. Power-up Boot Mode in "normal OS". Functions the same as when key is in local.

4.4 SPU and 3800 powered down. Power-up Boot Mode in "alternate OS" Functions the same as when key is in local.

Al,

3.43.2 CXTS - Convex Xpert Troubleshooting System

For a couple of years now,CONVEX has been developing an expert system based diagnostic tool, for the C3800. This product is called CXTS (CONVEX XPERT TROUBLESHOOTING SYSTEM). Previously this product was known as CATALYST, but has undergone this name change.

This product has made its way to alpha test (in-house) and will soon be going into beta test. The beta test sites have already been selected, so if you are not aware of it, then your particular site was not included.

The purpose of CXTS is to use its data base and rules to make decisions and suggestions to be followed after a system event. In many cases, its operation will be totally automatic. In previous tech bulletins and by fax, rules and flow charts have been sent to the field, detailing exact steps to take for specific extractor failures. These rules were part of CXTS and should give a good insight into the overall intent.

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The following modules are part of CXTS:

System picture files (detailed pictures of system components)
Online documentation (Includes removal and replacement instructions)
Document viewer User Interface (cxts_ui)
daemon (cxts_rt)
System configuration file (SCF)
History Database
Journal files
cxts_server
interface for errlogd
SPU daemons
System, I/O and scan based diagnostics

It is currently anticipated that CXTS will be available as a production release during Q193. During the next few weeks more detailed information will be made available about this product. So that by the time of its release, everyone should be aware of its functionality and operation.

The current prerequisites for CXTS is 3.2 diagnostics and 3.1.1 SST.

Al,

3.43.3 SPUOS 2.0 Upgrade and Repartitioning the Disk

During the recent SPUOS 2.0 upgrade on the OPUS/Cadd, the instructions called for repartitioning of the SPU disk. This repartitioning was not necessary for that particular upgrade and may have been bypassed during that upgrade.

It is very important, for future releases and new products that this disk repartitioning be accomplished. If for some reason this step was omitted from the upgrade, it is strongly suggested that a time be set up with the customer to perform this.

As all new releases of diagnostics and new products are based on the knowledge that all disks have been repartitioned, it is quite possible that any future upgrade can become a major problem.

Al,

3.43.4 C38 Error Message - init_commregs

The following error messages have occurred during the boot process, of a C3800:

init_commregs: error clearing comm reg 0xc lock
init_commregs: error clearing comm reg 0xd lock
init_commregs: error clearing comm reg 0xe lock
init_commregs: error clearing comm reg 0xf lock

From first appearance, it would appear that this is a hardware problem. But in several, recent, cases the problem has occurred as a result of extended troubleshooting and was ultimately cleared by reloading the diagnostics.

The actual mechanism that leads to this situation is not clear, but if this error is encountered and cu4000 executes with no failures then reloading the diagnostics should be the first step.

Al,

3.43.5 C3400 Spares Matrix - Revised

C3400 SERIES BOARD SET

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
410-002223-200	SP5	x	x	x
410-003224-200	PI2	x	x	x
410-001235-200	CUJ, Note 1	x	x	x
410-002235-200	CUJ, Note 2	x	x	x
410-002236-200	JCPU	x	x	
410-003236-200	JCPU	x	x	
410-004236-200	JCPU			x
410-005236-200	JCPU			x
410-003180-200	JSM System Monitor	x	x	
411-001340-200	SM2 System Monitor	Note 3	Note 3	x
410-002230-200	MCM3 without DMM's	x	x	x
411-000204-200	2mb DMM	x	x	x
411-001204-200	8mb DMM	x	x	x

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C3400 SERIES CABINET PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
411-002222-200	Fan Fail Sense board	x	x	
411-001339-200	Fan/environmental Sense			x
550-000009-290	Cartridge Tape Drive, 150mb	x	x	x
500-000250-200	Temperature probe assembly, inlet air	x	x	x
500-000251-200	Temperature probe assembly exhaust air	x	x	x
411-001221-200	Fan AC power distribution board	x	x	
604-080001-200	Delay line cable assembly		x	
604-160001-200	Clock line cable assembly		x	
411-000158-200	SPU disk paddle board assembly	x	x	x
411-000276-200	MEM_TOP Term Card	Note 4	Note 4	Note 5
411-000277-200	MEM_BOT Term Card	Note 4	Note 4	Note 5
411-000278-200	PI2_TOP Term Card	x	x	x
411-000279-200	PI2_BOT Term Card	x	x	x
411-001354-200	C3400-EX CPU Terminator Card			Note 6
204-000022-200	SPU disk, 477mb	x	x	x
500-000347-200	Blower Assy, Fn-2, Fn-4	Note 7	x	
500-000348-200	Blower Assy, Fn-1, Fn-3, Fn-5, Fn-6		x	
500-000383-200	Blower Assy, I/O and Memory areas			x
500-000384-200	Blower Assy, CPU Areas			x
500-000355-200	Blower sensor			x

C3400 SERIES POWER SYSTEM PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
500-000338-290	Power supply, -2vdc, 800w	x	x	
500-000338-291	Power supply, -4.5, 1800w	x	x	
500-000338-292	Power supply, +5vdc, 2000w	x	x	
500-000339-290	Power supply, multivolt 1000w	x	x	
500-000339-295	Power supply, multivolt	x		
500-000369-200	Power Controller - Domestic		x	
500-000367-200	Power controller - International		x	
500-000381-290	Power controller - Universal	x		
500-000218-200	Indicator panel - Domestic		x	
500-000218-202	Indicator panel - International		x	
500-000415-201	Power controller - Universal			x

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C3400 SERIES POWER SYSTEM PART NUMBERS

PART NUMBER	DESCRIPTION	Used In C3400-ES	C3400	C3400-EX
500-000438-200	Power supply, -2v 800w			x
500-000438-201	Power supply, -4.5v 1800w			x
500-000438-202	Power supply, +5v, 2000w			x
500-000439-200	Power supply, multivolt, 1000w			x
500-000533-200	Transformer, blower step-up, 60hz			x
500-003131-200	Processor control panel assembly			x

C3400 = Four head chassis |
C3400-ES = Two Head chassis |
C3400-EX = Eight head chassis |

Note 1: Required for Realtime systems

Note 2: Standard C3400 systems only. No support for Realtime systems

Note 3: Can be used in C3400-ES and C3400 with appropriate firmware. |
ROM part number 181-030041-107 used for C3400-ES and C3400 cabinets
ROM part number 181-030044-104 used for C3400-EX cabinets

Note 4: C3400 and C3400-ES use assembly revision A.0

Note 5: C3400-EX uses assembly revision B.0

Note 6: This terminator is required on a C3400-EX in any slot that does not have a matching CPU board installed. E.G. if a CPU board is installed in CPU-4 and no CPU is installed in CPU-5, a terminator card must be installed in the CPU-5 slot.

Note 7: Used for all fan locations in C3400-ES

A '|' in the right column indicates a change from the last release.

David Muir

3.44.1 env Utility and 10.0

In OS releases prior to 10.0, a utility existed in /mnt/os, at the spu, that allowed the display of environmental conditions associated with the mbus and vmebus chassis'. This utility existed as a link to the utility "dumpccu", which is also in /mnt/os.

Because the new products, excluding Javelin, are incapable of using this utility, the link was dropped for OS 10.0 and above.

For anyone desiring to use this utility, it is still possible to manually link dumpccu to env. It will still function as before.

For anyone not familiar with the "env" utility, an example of the output provided is shown:

MB0: +5V= 4.90 -5V=-4.90 +12V=12.05 -12V=-12.05 TEMP=30.67c (87.20f)
MB1: +5V= 4.90 -5V=-4.90 +12V=11.95 -12V=-12.00 TEMP=39.37c (102.86f)

The format of the command is env <-ccu#>. The command can also be executed from the OS by the use of "spucmd".

The command is valid for VIOP's and IOP's only and should not be used for other CCU types.

Al,

3.44.2 Potential epont Problem on C3800

There is growing evidence to suggest that the epont connectors, used in the C3800, may be experiencing stress, due to vibration, heat and other factors that may contribute to connector associated failures.

There is a possibility that the epont retaining screws may back out over time and break the seal, allowing contaminants to work between the fuji poly and backplane connection. This situation can lead to intermittent and widely scattered crossbar related failures.

Because this possibility exists, it is recommended that all eponts be checked to verify proper torque as soon as practical for each system. If any loose connectors are discovered, it is requested that this information be relayed to hardware support.

This situation is, not yet, deemed critical and should be considered a preventive maintenance item.

Al,

3.44.3 Crashdump -H on C3800

In order to execute a crashdump -H on a C3800, from /mnt/os, it is necessary to add /diag/hw to the PATH entry in /mnt/os/crashdump.

A standard crashdump that does not call hwdump will execute from /mnt/os, but if a hwdump is required, then it will be necessary to add this to the path, or execute crashdump from /.

An example of the current path as seen in the crashdump file:

```
#!/bin/sh

PATH=:.:/mnt/os:/bin:/mnt/bin
export PATH
```

Al,

3.44.4 dev_fddi.t Subtest 4050 Failure

Diagnostic dev_fddi.t will fail subtest 4050, on C2 class systems, with SP2's below rev R. The diagnostic will complete successfully with SP2's of rev R and above, or SP4 installed.

Subtest 4050 is designed to verify that the FDDI controller can receive packets to addresses stored in the content-addressable memory (CAM). This is similar to an address translation buffer.

Al,

3.44.5 C3800 Diagnostics 3.0.0.6

With the release of 3.0.0.6 diagnostics, the osc_update utility in /diag/db has been deleted. This is due to an effort to fix the nominal clock output at boot. This will obsolete the article 8 of chapter 3 in the C3800 Troubleshooting Guide.

In order to change the clock frequency under 3.0 diags, it is necessary to accomplish:

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put osc_freq x <where x is a value from 0-2>

0 = nominal	16.7ns
1 = lower	18.0ns
2 = upper	15.5ns

To display the current clock value a get of osc_freq will produce the following display:

```
VALUE: 16#00000000
|31|30|29 | 28 # 27 | 26 | 25 | 24 # 23 | 22 | 21 | 20 # 19 | 18 | 17 | 16
|                                Reserved                                |  spare
|15|14|13 | 12 # 11 | 10 |  9 |  8 #  7 |  6 |  5 |  4 #  3 |  2 |  1 |  0
|                                Reserved                                |   osc
```

It is important to remember that a diaginit, or a reboot of the Opus will return the value of this register to 0.

Al,

3.45.1 C3800 init_commregs Error Messages

In a previous release of the tech bulletins, the failure indication below was mentioned. In this bulletin, which is also in article 33 of chapter 3, in the C3800 Troubleshooting Hints.

init_commregs: error clearing comm reg 0xc lock
init_commregs: error clearing comm reg 0xd lock
init_commregs: error clearing comm reg 0xe lock
init_commregs: error clearing comm reg 0xf lock

Again, this failure will only be seen at boot.

The previous information indicated that the mechanism of failure was unknown, but the solution was to reload diagnostics.

It is now known that the failure mechanism is a jammed data base and can be cleared with the following procedure:

```
sys_shutdown
cd /diag/db
rm cdb.db* cdb.map* rb_*
kill_by_name cdb_startup
```

This procedure will remove the current database files, kill the current cdbserver and rbserver processes and restart them.

With everything that is now known, this should clear the problem with a minimum of trouble and effort.

Al,

3.45.2 C3800 Intermittent swis Errors

It has, very recently, been discovered that the swis is experiencing a very intermittent and so far, minor symptom.

It appears that when powering up the system with diaginit, that the swis will complain that a specific uart channel is missing. In most cases the uart channel will be for bay 6, which is a test loop on the swis itself and therefore of little consequence.

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But, there is a possibility that the failure can occur with an active bay; particularly bay 4 and thus prevent this bay from coming up. If this should happen, it is possible to clear the failure by executing the UART related subtests (213 and 214) in spu4000.

At present, it is felt that the problem is timing related with the spu and a solution is being investigated.

An example of the failure indication is shown below:

Sep 2 19:21:18 neptune_spu savecore: reboot after panic: parity error
Sep 2 19:21:46 neptune_spu vmunix: bpc: interlock found on uart channel(0)
Sep 2 19:21:46 neptune_spu vmunix: bpc:interlock found on uart channel(1)
Sep 2 19:21:46 neptune_spu vmunix: Swis:interlock changed interrupt received and not caught
Sep 2 19:21:46 neptune_spu vmunix: bpc: interlock found on uart channel(2)
Sep 2 19:21:46 neptune_spu vmunix: bpc: interlock found on uart channel(3)
Sep 2 19:21:46 neptune_spu vmunix: swis: interlock changed interrupt received and not caught
Sep 2 19:21:46 neptune_spu vmunix: bpc: interlock found on uart channel(4)
Sep 2 19:21:46 neptune_spu vmunix: swis: interlock changed interrupt received and not caught
**********uart channel (6) missing**********
Sep 2 19:21:46 neptune_spu vmunix: bpc: interlock found on uart channel(7)
Sep 2 19:21:46 neptune_spu vmunix: swis: interlock changed interrupt received and not caught

Al,

3.45.3 C3400 Parts Matrix Correction.

Please correct one line in the C3400 parts matrix that was in the last tech bulletin.

The part number for the control panel is:
500-003131-200 Processor control panel assembly

The part number should be:
500-003113-200 Processor control panel assembly

* Dave Muir *

3.45.4 C3400 Clock Tune Failures

Some C3400 processors exhibit a failure to load and verify the gate array clock tune values when the machine is first powered on. If you have V1.3 or higher of the C3400 system diagnostics/database installed, the boot operation will not continue if the clocks do not get loaded correctly. If the clocks do not load correctly and you attempt to boot the machine, other failures will happen during the boot process. If the CPU that failed to load clocks correctly is CPU-0, mminit will fail. If it is not CPU-0, then other failures may happen during autoconf, or possibly not until the system is at the OS.

If you have a system exhibits this problem after being powered up, allow the system to warm up for about 5 minutes before attempting to boot. After allowing the system to warm up, re-start the system with /etc/reboot and start from the 'fp>' prompt. Do not power the system back down.

An alternate method is to issue the following commands at the spu prompt:

load_clk (watch the output on the console to see if the clocks verify correctly. If they do not verify, try a second load_clk. If they fail to load and verify correctly a second time, the cpu board is defective.)

initall (This is REQUIRED after a load clock. Failure to run the initall will cause other scripts to fail during the boot.)

* Dave Muir *

3.45.5 C3400 Diagnostic/database Upgrade to 1.3 or 1.4

After loading Processor Diagnostics V1.3 or V1.4 in place of earlier versions of diagnostic/database software, it is necessary to re-boot the SPU before attempting to boot the system.

Failure to re-boot the SPU will result in a failure during mminit.

* Dave *

3.46.1 Updating a C3800 Data Base

As with other CONVEX systems, it is possible to add a new board and part number to the data base, on a C3800. The approach is somewhat different though.

The file to be edited is /diag/db/part_numbers. It is very similar to the file DB_cop, on a C2. But in order to get the part actually included in the data base, it is necessary to execute the command "add_parts". This will take any new entries in the part_numbers file and move them to the configuration data base. If no changes are necessary then "add_parts" will respond with "no new part numbers were found".

If the "add_parts" command is not executed, then the board will not be available until the SPU is rebooted. At a reboot the new part number will be added to the data base.

An example of the part_numbers file is shown below:

```
410-001149/viop/1&1:A-A,ZZ-ZZ;&
410-001269/tli/1&1:A-A,ZZ-ZZ;&
410-001228/idc/1&1:A-A,ZZ-ZZ;&
410-001328/hpi/1&1:A-A,ZZ-ZZ;&
410-001132/hsp/1&1:A-A,ZZ-ZZ;&
410-002132/hsp/1&1:A-A,ZZ-ZZ;&
411-000243/mc/0&
411-001243/mc/0&
411-002243/mc/0&
411-004243/mc/0&
411-005243/mc/0&
411-006243/mc/0&
500-001252/xbp/0&
500-001253/ccubpl/0&
500-001254/ccubpr/0&
411-001272/wi/0&
500-001251/iobp/0&
500-003251/iobp/0&
500-001286/cbpl/0&
500-002286/cbpl/0&
500-001287/cbpr/0&
500-002287/cbpr/0&
```

....continued on next page.....

410-002149/viop/1&1:A-A,ZZ-AA;&
416-001244/ia/1&0:A-0,ZZ-ZZ;&
416-003244/ia/1&1:B-0,ZZ-ZZ;&
416-004244/ia/1&2:B-0,ZZ-ZZ;&
416-001246/mb/1&0:A-0,ZZ-ZZ;&
416-003246/mb/1&1:A-0,ZZ-ZZ;&

Al,

3.46.2 VIOP Memory Page Allocation

We are starting to see a rash of situations that involve installing too many controllers on VIOP's due to page allocation. It is important to understand that, only, 128 memory pages are available on the VIOP and each controller uses a portion of this. The problem is getting serious, but is being pursued by development.

The present pursuit is to allow for dynamically allocating drivers, which will eliminate the need to load and link all of the drivers simultaneously. Thus saving large amounts of memory.

It has been suggested that the RTVIOP can be used to solve the current situation, but although this board has twice the memory installed, there is no software support for it available and the estimates for resources to accomplish this are considered too high, at present.

In the mean time it is important to understand that the majority of VME chassis installed, are already at, or near the limit. It is not practical for CONVEX to donate solutions to this problem, so in most cases the solution will be for the customer to remove controllers. This can be quite painful and avoided by proper analysis before selling a new controller.

In a pinch, for reduced cost to the customer, it is possible to drive one VME chassis with 2 VIOP's.

As a refresher, the memory usage for each controller (OS 10.x) is shown below:

EGOS	9
text data	50
text data w/Ultra	55
FDDI	7
ACM-201	14
DKC-203	4
DKC-204	4

.....continued on next page.....

LAN-007	11
tuned=3	9
tuned=2	7
tuned=1	5

*NOTE: With the ethernet patch installed, the memory usage becomes 17 pages and is no longer tunable, as only a single process is executed in this new driver.

LAN-202	5
LAN-204	1
MTC-201	14
MTC-201	15

It is important to CONVEX and our customers that we get the current situation under control.

Al,

3.46.3 Installing an ITC in C2 and C3 Series Systems.

There has been some confusion regarding the installation of the ITC on the C2 and C3 series systems.

The ITC is actually a respun IDC, part number 410-002228-200. In fact the data base will even consider this an IDC, even if used as an ITC.

The only support for ITC, on a C2, or C3400, is contained in the Diagnostic I/O release 1.1. It will not help to add the part number to the DB_cop file, as it will still fail the scn_link.

For a C3800 with 3.0.0.6 diagnostics, it is possible to add this to the data base. It is included in the database in future releases of diagnostics.

Al,

3.46.4 VBCU Part Number Change

In order to reduce costs, all returned VBCU's, part number 410-001150-200, will be upgraded, during the repair process, to RTVBCU's, part number 410-002150-200.

The RTVBCU was developed to provide the addition interrupt support required by the RTVIOP, but is completely compatible with the standard VIOP.

.....continued on next page.....

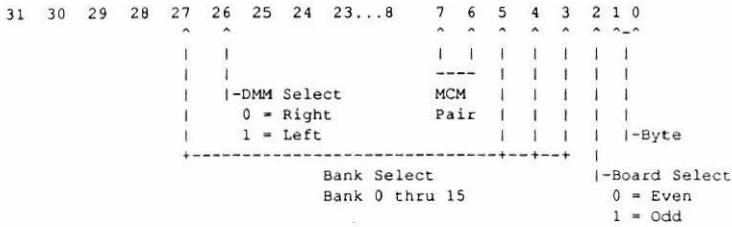
This does NOT announce a field upgrade program, as there is no additional functionality, but only informs the field that the 1150 will be modified to the 2150 VBCU, during the repair of returned boards.

Al,

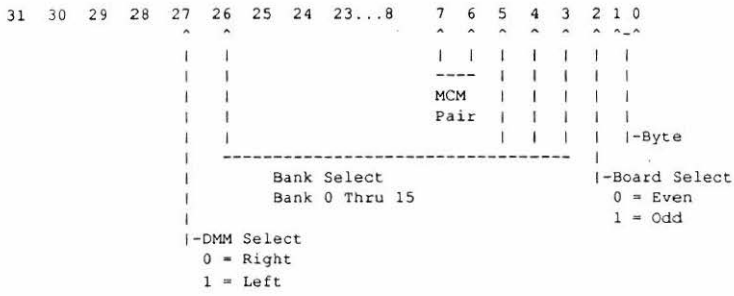
3.46.5 MCM-3 Memory Address Decoding Tool

Here is a tool that may help in decoding MCM-3 dmm locations. There is room at the top of chart to write down the hexadecimal address and convert it to binary along the top of the applicable DMM size.

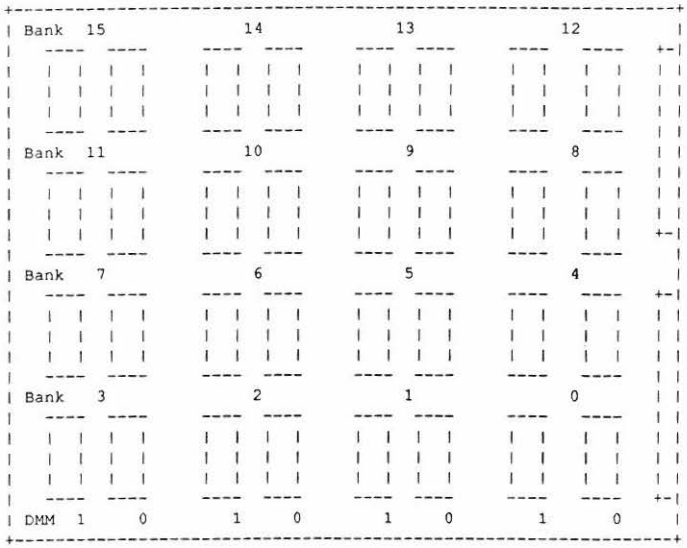
MCM-3 DMM Decoding With 8mb DMM (411-001204-200 - drams with 4400 in PN)



MCM-3 DMM Decoding With 2mb DMM (411-000204-200 - drams with 256 in PN)



.....continued on next page.....


Bank 15
14
13
12
Bank 11
10
9
8
Bank 7
6
5
4
Bank 3
2
1
0
DMM 1 0
1 0
1 0
1 0
CONNECTOR

* Dave Muir *

3.47.1 VME Versatec Controller VIOP Pages

The VIOP memory pages utilized, in 10.x, by the VME versatec controller, VPC-001 is 4 pages.

This information should be added to the table previously sent in the tech bulletin v3w46.

Al,

3.47.2 Power Plugs on C3400 and C3400-EX International Systems

Effective immediately, international shipments of C3400 and C3400-EX systems will not have a power plug installed.

* Dave Muir *

3.48.1 No Bulletin Information This Week

3.49.1 VIOP Pages Update

In a previous tech bulletin (v3w46, article 2) a mistake was made in the text size requirements for 10.x. The proper values are given below. Sorry for the inconvenience this may have caused.

In addition, it has come to light that the SCSI related patches, 10.1.128 and 10.2.128 use one extra page. This means that the MTC-201 and MTC-202 controllers will use 15 and 16 pages, respectively, when this patch is installed. This patch is included in 10.1.2 and production 10.2.

EGOS	9	
text data	55	
text data w/Ultra	60	
FDDI	7	
ACM-201	14	
DKC-203	4	Add one page for each disk over one
DKC-204	4	Add one page for each disk over one
LAN-007	11	
tuned=3	9	
tuned=2	7	
tuned=1	5	

*NOTE: With the ethernet patch installed, the memory usage becomes 17 pages and is no longer tunable, as only a single process is executed in this new driver.

LAN-202	5	
LAN-204	1	
MTC-201	14	15 pages with SCSI patch
MTC-202	15	16 pages with SCSI patch
VTEC	4	

Al,

3.49.2 C3800 ECC Timed Backoff Error Message

The memory messages, shown below, occur as a result of the system trying to throttle the single bit memory errors, to avoid swamping the soft log.

The total explanation follows:

.....continued on next page.....

Single-bit memory error data is stored in the CDB. Single- bit memory errors are isolated to the memory chip level. A count of total soft errors for each failed memory chip is maintained. By default, errintd will store a maximum of 60 memory chip entries in the CDB.

Once the number of total memory chip failures reaches 75% capacity and a burst of errors occur (e.g., at a rate of 1 every 10 seconds), the logging of new chips in error is throttled, or governed, to prevent the log from immediately reaching its capacity. Whenever throttling occurs, a message is written to the console.

```
Loading vmunix
mm_sniff: sniff rate: 32.14 MB/day (7.90 days/pass)
errintd: Soft ECC timed backoff(1): 0.750 secs.
errintd: Soft ECC timed backoff(2): 0.750 secs.
errintd: Soft ECC timed backoff(3): 0.750 secs.
errintd: Soft ECC timed backoff(4): 1.000 secs.
errintd: Soft ECC timed backoff(5): 2.000 secs.
errintd: Soft ECC timed backoff(6): 5.000 secs.
errintd: Soft ECC timed backoff(7): 20.000 secs.
```

These errors will frequently be reported at boot, when a memory board has been powered off and left installed. As previous tech bulletins have indicated, a powered down memory board must be physically removed from the system.

In addition, a nmc failure can result in the same output.

Al,

3.49.3 C3800 Head Offline When Rebooting

It should be understood that if a head has been removed from the OS configuration, by the APR function, then this head will be off-line when the system is rebooted. This is because the current process clears the cpu_os_req field, for the head, in the database.

This problem will be corrected with the next diagnostic release, which is due in early January.

In the meantime, the safest solution is to insert a cpuconf at the bottom of the .login file, so that on a reboot the available heads will be displayed, which should remind the customer to re-enable the head.

Al,

3.50.1 C3800 spuio Problem

A problem with the spuio link between the 3800 and the spu is, currently, being experienced. The failure manifests itself as a spu I/O error at the CONVEXOS level when attempting to accomplish spu commands. Quite often, though not always, this will be accompanied by a swip bus error.

The cause of the failure is not known, at this time, but customers should be discouraged from initiating heavy activity with this link.

In the mean time, it is requested that the spuio process be killed and restarted at the SPU level. This can be accomplished by the following command sequence.

```
kill -9 pid
spuio &
```

It is not certain that this will restore the link, but should be attempted.

This only affects the link from the 3800 to the SPU and does not impact the link from the SPU to the system. This failure will result in the failure of the APR mechanism and will eventually lead to system hangs, if not detected and fixed.

Al,

3.50.2 C3800 ARP Script

In order to initiate the apr process and start the cpu_monitor daemon, it is important that the following script be inserted into the bottom of the rc.local file. Any mistakes in this entry will lead to the process not starting and therefore not executing APR.

```
if [ -f /etc/cpu_monitor -a -f /etc/cpu_monitor.config ]; then
    /etc/cpu_monitor &
    echo -n ' cpu_monitor'
fi
```

Again, any inaccuracy in the entry will lead to cpu_monitor not starting. There will be no error printed to indicate this. It can only be verified by monitoring the message at boot, or executing a ps.

Al,

3.50.3 C3800 CCU Temperature Sensors

It has been found that the CCU Temperature Sensors do not use the "front facing" concept when reporting temperature warnings. The following is an example of a Hot BPC Temperature message. As can be seen, the below message is reporting the problem for the RightCCU Outlet. The Right-CCU Outlet is the one on your right as you are facing AWAY from the cabinet. It was verified that messages reported for the LeftCCU Outlet will be on your left facing AWAY from the cabinet.

```
*******************************************************************************
+++>
<Wed Nov 11 15:14:18 1992>   /diag/bin/bpcwatchd(245):../bpcwatchd.c:164
Env Error (DiagER350): message received by SPU

BPC: 4              BAY: UNKNOWN
PPC: UNKNOWN        SLOT: UNKNOWN        TARGET: UNKNOWN
BPC MSG:      REPORTED HOT BPC TEMPERATURE
RightCCU Outlet

msgid:82 length:08 source:08 nwi_uart:04 misc0:00 misc1:00 group:72 error:40
@BPC= 4             @BAY= UNKNOWN        @MSGID= 82   @GROUP= 72  @ERROR= 40
@PPC= UNKNOWN       @SLOT= UNKNOWN       @TARGET= UNKNOWN
****

+++>
<Wed Nov 11 15:14:18 1992> /diag/bin/bpcwatchd(245):../bpcwatchd.c:164
Env Error (DiagER350): message received by SPU

BPC: 4              BAY: UNKNOWN
PPC: UNKNOWN        SLOT: UNKNOWN          TARGET: UNKNOWN
BPC MSG:      REPORTED WARM BPC TEMPERATURE ON SENSORS:
RightCCU Outlet

msgid:82 length:08 source:08 nwi_uart:04 misc0:00 misc1:00 group:81 error:40
@BPC= 4             @BAY= UNKNOWN        @MSGID= 82   @GROUP= 81  @ERROR= 40
@PPC= UNKNOWN       @SLOT= UNKNOWN       @TARGET= UNKNOWN

*******************************************************************************
```

Jerry

3.51.1 C3800 Crashdump Validity Problem

It has been discovered that many of the C3800 SPU based utilities and interactive tests invalidate the validity of a crashdump. For this reason it is recommended that no SPU based utilities be considered if it is felt that a crashdump will be necessary to pursue the problem.

These utilities would include:

rslog	xbar_err	pb_walk	idc_con
syscon	xbinteg	xc_con	nmb_errs
ncutestall			

Other utilities should cause no harm.

Al,

3.51.2 Most Frequently Reported Failures

As promised, below is a list of the most frequently reported failures. This list is across all product lines and is listed by the severity of the impact. Although there are certainly other problems, these have the most severe impact on our customers:

1) VIOP MEMORY Restrictions
2) MCM3 (C2, 3400) configuration memory failures. This includes decoding locations and memory upgrades.
3) C3800-SPU link
4) C3800 nvrf2 failures
5) Sysgen failures (All systems)
6) Wrong Answers/Job aborts (All systems)
7) FDDI installations
8) Crashdump failures (All systems)
9) C3800 NCU failures. This includes clock, power and STRAM causes
10) C2 RITA failures
11) C3400 related PI failures
12) IPI disk failures
13) C3800 STRAM
14) C3400 System Hangs while looping on dsi

This list will be updated approximately once a quarter, as it usually takes this long to change the list substantially.
Al,

3.51.3 C3800 SPU and idcfmt problem

It should be understood that it is, currently, not possible to successfully execute idcfmt on the SPU of a C3800 system. It will be necessary to format all IDC drives at the ConvexOS level.

This problem has been resolved in the 3.3 Diagnostic release, which has been released and can be expected to begin shipping within 2 weeks.

Al,

3.51.4 Wrong Memory Address Reporting by errintd

When logging soft errors, errintd is reporting the wrong memory board of the memory pair. The memory board reported is always the 'even' board of the pair.

All the other information relating to the bank and dmm in the log entry is correct.

Until this problem is corrected, it is suggested that the dmm on both the even and odd memory boards be changed, since there is not way to tell which board has the failing dmm.

* Dave Muir *

3.52.1 No Bulletin Information This Week.

4.1.4 Using C3800 Extractors to Isolate Intermittent Failures

Quite often it is necessary to pursue an intermittent system failure, on a 3800, without benefit of a supporting diagnostic failure. In these situations the only information available is that obtained from the hardlogger. This information generally consists of the extractor, port, and the data, or address involved.

After determining the source and destination of the data, or address, the solution will ultimately be based on determining the data in error. As the problem is unknown and can be anything from connectivity to a failed component, it is important that the failed data be analyzed as thoroughly as possible.

In most cases the usable information will consist of a failed byte and the parity for this byte. An example can be seen below:

```
HARDERROR #      BOARD TYPE        PORT/SIDE       EXTRACTOR
-----------      ----------        ---------       ---------
    1             SP_TYPE             3          sp_nrc.xro_stop_in
```

```
sp3;nrc0.par_err_stop_in = 1 \
sp3;nrc1.par_err_stop_in = 1 |  These should all have the same value
sp3;nrc2.par_err_stop_in = 1 /
    Parity error script for xro_data
       bus received by NRC0, NRC1 and NRC2 gate arrays
  Register name          Ring value              Board signal name
 ------------------------------------------------------------------------
  xro_data<>          00  00   6a   c1           XRO_DATA<31..0>
  xro_data<>           1   1    1    1*          XRO_PAR<0..3>
  *indicates parity error
```

As can be seen, in this example, the error has occurred in byte 0 of the data, but this may not be enough information. Especially in cases where an intermittent connectivity failure is involved, this byte may involve up to 3 eponts and 4 augats, so it is important that the specific bit be determined to permit further scrutiny and monitoring. This will lead to the quickest solution.

The best tool, available, to locate the actual bit is the return control que (rcque). Often, through close examination, the failed data can be located and in these cases the lost bit can be determined.

Below is an example of the rcque output and close examination shows that the data word we are searching for is most probably located in location d of the que output. This data is 00006ac3, this would suggest that the failed bit location is at bit 1. This further isolates the failure and reduces the

.....continued on next page.....

area to be searched. Also insure that the data matches with the extractor. IN other words, in this case, odd data is required.

```
[DDB]-> $dcpu 1
[DDB]-> $rcque

                CPU1 Dump of the RETURN CONTROL QUEUE
    ------------------- SP1 return control queue ----------------------
   ptr  dest size reg tag eo P    addr        ptr P odd_data       P evn_data
   --- ------ --- --- --- -- - --------      --- - --------       - --------
    00   vp-1  2   03  1e 10 8 8015ab50       00 8 2e2c3e5d       0 ae67f4d6
    01   vp-1  2   03  1f 10 0 8015ab58       01 3 ae45b20f       a 2e6d28b0
    02   vp-1  2   03  01 10 8 8015ab60       02 e 2d87deae       3 ae37deaa
    03   vp-1  2   03  02 10 0 8015ab68       03 8 af2092ec       9 ac919d48
    04   vp-1  2   03  03 10 0 8015ab70       04 3 2f4c4eb8       3 ad13e200
    05   vp-1  2   03  04 10 8 8015ab78       05 c af6c3804       5 ae489b00
    06   vp-1  2   03  05 10 0 8015ab80       06 3 2f850f35       8 2dd370f8
    07   vp-1  2   03  06 10 8 8015ab88       07 c af81d54c       3 adad9ab4
    08   vp-1  2   03  07 10 8 8015ab90       08 7 2f3a5372       e 2dc0cc6e
    09   vp-1  2   03  08 10 0 8015ab98       09 3 aed903b4       f 2e24ac36
    0a   vp-1  2   03  09 10 8 8015aba0       0a f 00000000       7 ae442d84
    0b   vp-1  2   03  0a 10 0 8015aba8 r/w>  0b 6 2f2ee84c       a 2dd6a607
    0c   vp-1  2   03  0b 10 0 8015abb0       0c 8 af1592e0       a af2af56e
    0d   vp-1  2   03  0c 10 8 8015abb8       0d f 00006ac3       5 2f42ce0a
    0e   vp-1  2   03  0d 10 8 8015abc0       0e 5 ae3acd9c       c af696b9e
    0f   vp-1  2   03  0e 10 0 8015abc8       0f 0 ada80802       5 2f82f860
    10   vp-1  2   03  0f 10 0 8015abd0       10 9 2d589828       8 af838532
    11   vp-1  2   03  10 10 8 8015abd8       11 7 ae55d4e1       5 2f3f32aa
    12   vp-1  2   03  11 10 0 8015abe0       12 e 2e849310       0 aedcdc32
    13   vp-1  2   03  12 10 8 8015abe8       13 4 ae0fc8ef       f 00000000
    14   vp-1  2   03  13 10 8 8015abf0       14 7 2c9c6528 r/w>  2 2f2f77bf
    15   vp-1  2   03  14 10 0 8015abf8       15 0 2c1aa880       f af1e65f5
    16   vp-1  2   03  15 10 c 8015ac00       16 6 ae1bb7a8       3 2f08a066
    17   vp-1  2   03  16 10 4 8015ac08       17 a 2e157d86       3 ae622bfc
r/w>18   vp-1  2   03  1d 10 8 8015ab48       18 3 adb03f3c       2 ae045a02
```

It should be understood that this information is only valid at the time of the event. So APR may have to be disabled in order to retrieve the correct entries.

By use of this tool, the FE is now able to concentrate, entirely, on a single bit. Without knowing the bit the search is much broader and with an intermittent may even result in failure.

Al,

4.1.5 Revised C3800 SPU Backup and Restore Information

The changes are in the restoring "/" section and are noted here:

```
# cd /a
Insert the "backup" tape in the DAT drive.
# mt -f /dev/rst0 rew
# restore xf /dev/rst0
.
.
Specify next volume#: 1
# Set directory mode, owner, and times.
set owner/mode for ".."? [yn] y
# cd /
# umount /a
# /etc/fsck /dev/rsd0a
# mount /dev/sd0a /a
^^^^^^^^^^^^^^^^^^ added this line
# cd /usr/kvm/mdec
# installboot /a/boot bootsd /dev/rsd0a
            ^^ added /a
# /etc/reboot
```

The complete procedure is listed below

Using Backup and Restore

Backup

The "/etc/backup" script looks at "/etc/fstab" to determine which file systems to dump.

Here is what "fstab" looks like on a SPU running SpuOS 2.0 and Diags 3.0.

```
/dev/sd0a / 4.2 rw 1 1
/dev/sd0f /diag 4.2 rw 1 3
/dev/sd0e /mnt 4.2 rw 1 4
/dev/sd0h /sst 4.2 rw 1 5
/dev/sd0g /usr 4.2 rw 1 2
```

.....continued on next page.....

"/etc/backup" will dump the file systems in the following order:

/
/diag
/mnt
/sst
/usr

Be sure to make note of the order the file systems are dumped, so you will have the proper info if you need to "restore" from the "backup" tape.

To backup the SPU do the following:

Insert a write enabled tape in the DAT drive.

spu> su to become root.
spu\> cd /
spu\> /etc/backup

This will dump all of the SPU file systems onto one tape.

Restore

Restoring "/"

At the ">b" prompt
Insert the "SpuOS" tape in the DAT drive.

>b b st()
Probing Memory.....
Booting from: st(0,0,0)

What would you like to do?
1 - install mini-root
2 - exit into single user shell
Enter a 1 or 2: 1
.
.
.
.

.....continued on next page.....

```
Do you want to format and/or label disk "sd0"?
1 - yes, run format
2 - no, continue loading miniroot
3 - no, exit into single user shell
Enter a 1, 2, or 3: 2

.
Problem with tape: what do you want to do?
1 - retry the tape "st0"
2 - use a different tape unit
3 - abandon miniroot install and enter single user shell
Enter a 1, 2, or 3: 1

.
Mini-root installation complete.

What would you like to do?
1 - reboot using just-installed miniroot
2 - exit into single user shell
Enter a 1 or 2: 1

.
You will see boot messages and then the miniroot prompt "#".

.
# newfs /dev/rsd0a
# mount /dev/sd0a /a
# cd /a
Insert the "backup" tape in the DAT drive.
# mt -f /dev/rst0 rew
# restore xf /dev/rst0

.
Specify next volume#: 1
# Set directory mode, owner, and times.
set owner/mode for ".”? [yn] y
# cd /
# umount /a
# /etc/fsck /dev/rsd0a
# mount /dev/sd0a /a
# cd /usr/kvm/mdec # installboot /a/boot bootsd /dev/rsd0a
# /etc/reboot
```

.....continued on next page.....

Restoring "/usr"

At the ">b" prompt
Insert the "SpuOS" tape in the DAT drive.

>b b st()
Probing Memory.....
Booting from: st(0,0,0)

What would you like to do?
1 - install mini-root"
2 - exit into single user shell"
Enter a 1 or 2: 1
.
Do you want to format and/or label disk "sd0"?
1 - yes, run format
2 - no, continue loading miniroot
3 - no, exit into single user shell
Enter a 1, 2, or 3: 2
.
Problem with tape: what do you want to do?
1 - retry the tape "st0"
2 - use a different tape unit
3 - abandon miniroot install and enter single user shell Enter a 1, 2, or 3: 1
.
Mini-root installation complete.

What would you like to do?
1 - reboot using just-installed miniroot
2 - exit into single user shell
Enter a 1 or 2: 1

You will see boot messages and then the miniroot prompt "#".

newfs /dev/rsd0g
mount /dev/sd0a /a
mount /dev/sd0g /a/usr
cd /a/usr

Insert the "backup" tape in the DAT drive.

.....continued on next page.....

```
# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 5
.
Specify next volume#: 1
# Set directory mode, owner, and times.
set owner/mode for ".”? [yn] y
# cd /
# umount /a/usr
# umount /a
# /etc/fsck /dev/rsd0g
# /etc/reboot
```

Restoring "/diag"

Boot the system to single user.

```
>b b -s
# /etc/newfs /dev/rsd0f
# mount /dev/sd0f /diag
# cd /diag
```

Insert the "backup" tape in the DAT drive.

```
# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 2
.
Specify next volume#: 1
set owner/mode for ".”? [yn] y

# cd /
# umount /diag
# /etc/fsck /dev/rsd0f
# ^d (Go to multi-user)
```

Restoring "/mnt"

Boot the system to single user.

```
>b b -s
# /etc/newfs /dev/rsd0e
```

.....continued on next page.....

```
# mount /dev/sd0e /mnt
# cd /mnt

Insert the "backup" tape in the DAT drive.

# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 3
.
Specify next volume#: 1
set owner/mode for ".”? [yn] y
# cd /
# umount /mnt
# /etc/fsck /dev/rsd0e
# ^d (Go to multi-user)

Restoring "/sst"

Boot the system to single user.

>b b -s
# /etc/newfs /dev/rsd0h
# mount /dev/sd0h /sst
# cd /sst

Insert the "backup" tape in the DAT drive.

# mt -f /dev/rst0 rew
# restore xfs /dev/rst0 4
.
Specify next volume#: 1
set owner/mode for ".”? [yn] y
# cd /
# umount /sst
# /etc/fsck /dev/rsd0h
# ^d (Go to multi-user)

Dan Brenner
```

4.2.1 ioconfig Entry for VME Exabyte 8mm Tape Drives

The following are the current /ioconfig entries for the VME version of the Exabyte EXB-8200 & EXB-8500 series 8mm tape drives. Both drives are identified by the same entry, with the exception of the unit number if drives are daisy-chained, as the differences between these units in tape capacity is a function of the drive and not the formatter.
Example:-

```
viop ?
  vme ?
    ctlr SBC-001 csr 0xFE00 int 6
      unit 0 type EBD-001
```

or:-

```
viop ?
  vme ?
    ctlr SBC-001 csr 0xFE00 int 6
      unit 0 type EBD-001
      unit 1 type EBD-001
```

-Kelvyn

4.2.2 Cluster Cabinet Site Prep

Currently the Site Prep Guide is not available for the Cluster Cabinet. If you need to configure electrical and A/C needs for a cabinet, please treat it as a fully loaded, with disk drives, EXP-105 HPP Cabinet.

The Site Prep Guide should be released in the near future.

Chris Magargee

4.2.3 Link Model MC5 Console Terminal

The new Link MC5 Terminal has been shipping as the C32XX or C34XX console. When a site receives one of these terminals, there should be a Users Guide with it.

.....continued on next page.....

The following is a quick reference on how to print a screen or toggle continuous print.

To print current screen depress at the same time, Shift-Print Send keys.

To toggle continuous print depress at the same time, Ctrl-Shift-Print Send keys.

More information on the actual configuration and setup of the terminal will be released in Gen-011 of TechTips, which should be out by the end of January.

Chris Magargee

4.2.4 3800 SPU Boot From Tape Problem

A problem has been discovered when booting SpuOS 2.0 from tape directly after power up. This problem should only arise when installing a new unloaded disk in a 3800 spu.

To work around this problem, do the following:

1. Insert a SpuOS 1.0 tape in the DAT drive.
2. At the ">" prompt type "n" <cr>.
3. At the "ok" prompt type "boot st()" <cr>.
4. At the "Boot:" prompt type "st(„4)" <cr>.
5. When you see the "Initialize ram disk from device:" question, press the "L1" and "a" key at the same time.
6. Insert the SpuOS 2.0 tape in the DAT drive.
7. At the ">" prompt type "b st()" <cr>.

You may then install SpuOS 2.0 according to the "C3800 Service Processor Unit Service Guide" 2nd Edition chapter 4.2.1 or restore SpuOS 2.0 according to Tech Bulletin Vol. 4 Week 1 Article 5.

I recommend all FE's, working on 3800's, verify they still have a copy of SpuOS 1.0 available. If you do not have a copy, send e-mail and I will get some made and shipped to you.

I will notify you when this problem has been resolved.

Dan Brenner

4.2.5 Change for V4W1 Article 5, C3 SPU

In Tech Bulletin V4W1 article 5, please change each occurrence of:

At the ">b" prompt to At the ">" prompt

and

>b b st() to >b st()

and

>b b -s to >b -s

I have already corrected the online (tacinfo) document. Sorry about that,

Dan Brenner

4.2.6 C3800 SST Failures

It is possible to experience a failure with SST, on an individual board, even though the board appears to function perfectly fine. In these cases the component that has failed, should still be replaced.

It is impossible to be sure what functions may be affected by the failed component and the board could be exhibiting subtle problems, such as wrong answers. In addition, if the failed component is located on a NSP, or NVP, in the case of a 3800, then APR will be unable to return the head to an online status.

The most predominant failures seen, that fit this description, is the NSP.

Again, the failing component should be replaced when a SST failure is encountered. This does not include cases where sst will not execute because a component is mis-copped.

Al,

4.2.7 Installing C3800 epont Cables

On initial 3800 installations, it is recommended that epont cables be installed first on the crossbar backplane and then to the CPU backplane, after the bay is mechanically connected to the central cabinet.

This means that all eponts would be installed on the crossbar for the bay. The bay would then be mated to the central cabinet and then the eponts connected to the cpu backplane.

The reason for this is when installing the eponts on the bay first and then mating to the central cabinet can cause an un-natural bend of the flex cable and therefore create a torque on the cables that can make them difficult to remove and eventually cause a defect.

There have been some recent epont failures where this method of installation may have contributed.

Al,

4.2.8 Crashdumps Needed for C3800 Failures

The following failure has become a major problem with 3800's. For this reason, it is urgent that we acquire crashdumps after these failures. The particular symptom is characterized by an exception of C01, or C04, as indicated in register A5.

```
[CPU00@19:08:53]. ConvexOS: FATAL ERROR: (arch,7036) Exception_handler: Not
enough context stacks
[CPU00@19:08:53]        sp:     001cce1c        a1:     001cdd90
[CPU00@19:08:53]        a2:     ffff4000        a3:     00000f50
[CPU00@19:08:53]        a4:     0000000b        a5:     00000c01
[CPU00@19:08:53]        ap:     001cce30        fp:     001cce1c
[CPU00@19:08:53]        s0: 000000000000007a    s1: 0000000000123be8
[CPU00@19:08:53]        s2: 30312c750000007b    s3: 00000000000005a2
[CPU00@19:08:53]        s4: 362c753234313031    s5: 33312c75112bac00
[CPU00@19:08:53]        s6: 30382c7532333230    s7: 30342c7532343130
[CPU00@19:08:53]        int. mask: 00000003
```

Al,

4.2.9 hwdump problem on C3400

A change was made with the release of V1.1 of the system diagnostics that changed the location of the UCODE_REV file. This caused a problem with hwdump. This also effects crashdump with -H option.

hwdump will run on systems that were shipped with V1.0 and later upgraded since the file /mnt/usr/ucode.2236/UCODE_REV will still exist. However, the incorrect version of microcode will be reported by the hwdump.

Here is how to correct the problem.

1. Make a copy of hw/cputest/hwdump
2. Edit the hwdump script and make the following change:

From: cat XxX.1 XxX.2 XxX.3 XxX.4 XxX.5 /mnt/usr/ucode.2236/UCODE_REV > $1

to: cat XxX.1 XxX.2 XxX.3 XxX.4 XxX.5 /mnt/usr/ucode/UCODE_REV > $1

This will be changed in the next release of the diagnostics.

* Dave Muir *

4.3.1 C3400 Series Power Information

There has been some confusion recently about power requirements and model numbers for the C3400 series systems. It is important to be certain about the model number you are planning for, since there are significant differences between models.

C3400 - (Javelin 4 head)
This is the first of the javelin series to ship. It has a maximum capacity of 4 CPU's, 8 memory boards and 6 IOP's, 2 PI-2 boards.

Power requirements:

North American	200-208 vac, 3 phase, 50/60 hz, 4 wire
International	240/415 vac, or 220/380 vac, 50/60 hz, 3 phase 5 wire Max CB rating 100 amp

Power connector:

North American	4100P9W plug attached 4100C9W receptacle for conduit 4100R9W receptacle for wall mount
International	No plug attached
Site Prep Guide - Processor Diagnostic Manual	DHW-221, 081-008930-000 DHW-302, 760-003830-000

C3400-ES - (Javelin Junior)
This is the second javelin model that was shipped. It has a maximum capacity of 2 CPU's, 2 memory boards and 3 IOP's, 1 PI-2. The system can have an internal VME chassis (model C3400-ES-cs) or be shipped with the internal chassis removed (C3400-ES).

Power requirements:

North American	200/220/240 vac, single phase, 50/60 hz
International	Same as North American Max CB rating 60 amp

.....continued on next page.....

Power connector:

North American	360P6 plug attached 360R6W receptacle for wall mount 360C6W receptacle for conduit mount
International	Same as North American
Site Prep Guide -	DHW-305, 081-018430-000
Processor Diagnostic Manual	DHW-302, 760-003830-000

C3400-EX (Javelin 8 Head)
This model uses the deep chassis that will support up to 8 CPU boards. The even numbered CPU's are in the front of the chassis and the odd numbered CPU's in the back of the chassis. Memory and I/O are the same as the C3400.

Power requirements:	200-208 vac, 3 phase 50/60 hz, DELTA or WYE ONLY
North American	If a WYE power source is used for North American systems, neutral is not used.
International	If 200-208 vac three phase power is not available, then a step-down transformer is required. A step-down transformer kit (Convex PN 550-003114-200) is available from Convex. The transformer kit includes a 560C9W receptacle.

Power connector:

North American	460P9W plug attached 460C9W receptacle for conduit mount 460R9W receptacle for wall mount
International	560P9W Plug attached 560C9W receptacle for conduit mount 560R9W receptacle for wall mount
Site Prep Guide -	DHW-308, 081-021330-000
Processor Diagnostic Manual	DHW-302, 760-003830-000

.....continued on next page.....

C3400/ESX - (Javelin 4 head)
This is a revised offering of the original Javelin 4 head chassis. The differences are cosmetic. All the specifications and requirements for this model are the same as the Javelin 4 head chassis.

* Dave Muir *

4.3.2 Verify cop on Initial Board Installation

It is recommended that the cop information be verified with all replacement boards, on initial installation. This is because there has been numerous occasions where the board replaced has been incorrectly copped and missed until a later date.

It should be understood that after copping a board, it is necessary to remove power from the board and execute diaginit, in order to recognize the new scan configuration. This is especially true for SST to function.

In addition, it is not possible to change the DC test ring directly, but is updated after the cop information has been entered during the copmod function.

Al,

4.3.3 Using SST on C3800

In cases where SST is inconclusive about what component a failure lies with, it can be very helpful to run SST on each failing component.

In the example below, it is obvious that the failures exist with the crossbar, but not clear as to the exact cause:

```
BOARD   PORT        % CHANCE OF    --- Single Board Failures --
NAME    NAME          FAILURE
xrt     XBARodd       100%
                            Total Single Board Failures: 1
BOARD   PORT        % CHANCE OF    --- Multi-Board Failures -n
NAME    NAME          FAILURE      --- Overlap Single Board --
xrt     XBARevn       37%
xrt     XBARodd       37%
xbp     XBAR          24%
                            Total Overlap Failures: 168
```

.....continued on next page.....

```
BOARD   PORT         % CHANCE OF    --- Multi-Board Failures --
NAME    NAME           FAILURE      --- No Overlap --
sp      port 5         31%
xrt     XBARevn        46%
xbp     XBAR           10%
cbpr    port 5         10%
                              Total Separate Failures: 2

--------> CURRENT FAILURE SUMMARY FOR TEST RUN <========----
BOARD   PORT         % CHANCE OF    --- Multi-Board Failures --
NAME    NAME           FAILURE
xrt     XBARodd        61%
xbp     XBAR           38%
```

In this situation it is quite easy to run SST individually on each of the possible failed components, in order to make a definitive diagnosis.

This can be accomplished by executing SST and entering the Configure Menu by entering a "1" at the SST prompt. The Configuration menu is shown below:

```
Configuration Menu

 1. display        display the current configuration
 2. hardware, -h   set configuration to installed hardware
 3. tape,     -t   set configuration to rings with networks on tape
 4. clear,    -c   clear the current configuration
 5. add,      -a   add scan rings associated with board
 6. remove,   -r   remove scan rings associated with board
 7. include,  -i   include rings
 8. exclude,  -e   do not include rings
 9. asm,      -m   force board assembly revision
10. wire,     -w   force board wire revision
11. part,     -t   force board part number
12. main          go to main menu
```

In this case a "-c" can be entered at the prompt, which will clear the current configuration. This will be followed by a "-i xxx", where xxx is the board to be tested. This will insert the specific module in the configuration. Then a return to the main menu and test execution should be accomplished.

As the menu method can be quite cumbersome, it is also possible to enter SST by way of a command line. This would be accomplished by the following method:

sst conf -c -i xxx <where xxx is the component to be tested>

.....continued on next page.....

This command will take you directly to the main menu where the test can be executed on this module.

By this method, it will be possible to verify the actual failed component and overcome the uncertainty created by the "%" display. Which as stated before, indicates the location percentage of nets tested and not the odds of a failure occurring on a specific module.

It would be useful to review article 13 of Chapter II, in the C3800 Troubleshooting Guide.

Al,

4.3.4 itc4000 Diagnostic Information

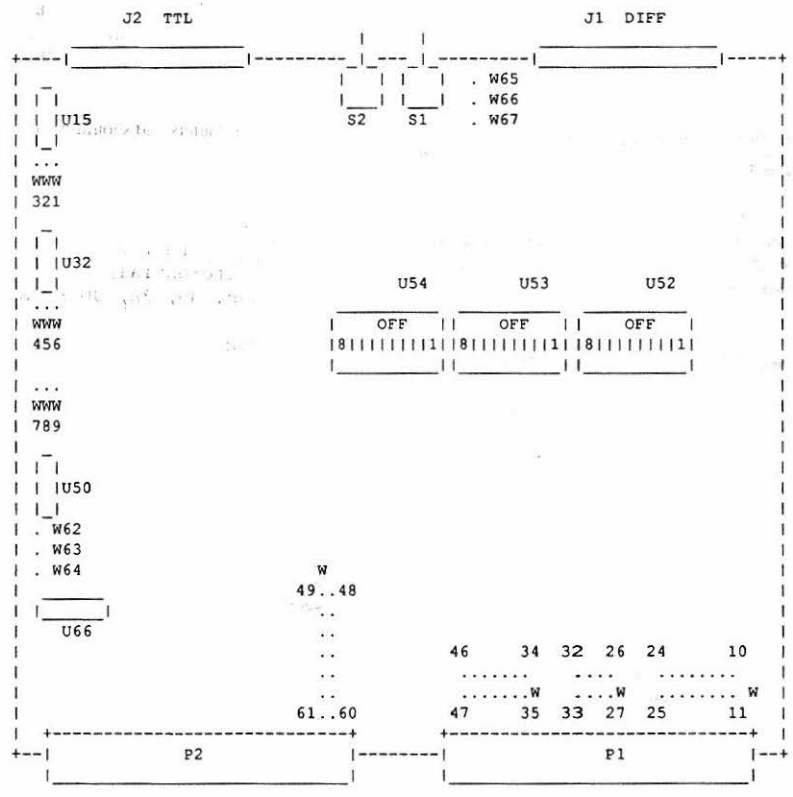
The diagnostic "itc400.t" is unable to distinguish the difference between an installed "idc" controller and an "itc" controller. This is important to remember if your system has both "idc" and "itc" controllers installed, and you need to run this diagnostic. When the diagnostic requests the "ccu" number to test you MUST specify the ccu slot number that contains the "itc" controller. The default of "0" DOES NOT correspond to the first "itc" controller installed, but to the first idc/itc type controller it finds.

-Kelvyn

4.4.1 VME IKON Configurator

The configurator for the VME Ikon I/F controller, contained in Tech Tip Gen 11, is incorrect with respect to the switch positions for U54. The correct configurator is shown below:

211-000111-200 Ikon 10088 VMEbus Hardcopy Interface Controller Configurator



.....continued on next page.....

The Controller Base Address is normally set to "0x100" using dip switches U54 (1-8), U53 (1-8) and U52 (1-4) according to the chart shown below. To select a Base Address other than the one shown below, add a multiple of 0x10 to the base address. For example, to add a second controller, set the base address on it to "0x110" by switching OFF U53-8 and U54-4.

BASE ADDRESS SWITCH SETTINGS (Address 0x100)

	1	2	3	4	5	6	7	8
U52	ON	ON	ON	ON	ON	ON	ON	ON
U53	ON	ON	ON	ON	ON	ON	ON	OFF
U54	ON	ON	ON	ON				

The upper half of U54 is also used to select some of the operational parameters and should be set according to the following chart:

DIP SWITCH	POSITION	PURPOSE
U54-5	ON	Set for 16 bit DMA transfers
U54-6	OFF	Send low order byte of halfword first
U54-7	ON	Use TTL interface (not differential)
U54-8	ON	Use address modifier codes: 39, 3A, 3D & 3E

The jumpers on the board should be set according to the following chart:

FROM	TO	PURPOSE
W2	W3	Standard option timing
W4	W5	BUSY signal interpretation
W7	W8	BUSY signal interpretation
W11	W13	Bus Grant Level #0 Bypass
W15	W17	Bus Grant Level #1 Bypass
W19	W21	Bus Grant Level #2 Bypass
W22	W23	Bus Grant Level #3 Input
W24	W25	Bus Grant Level #3 Output
W32	W33	Bus Request Level #3
W36	W37	Interrupt Request Level #6
W50	W51	Interrupt Acknowledge Level #6
W63	W64	Test pattern select
W65	W66	Enable selective Data Streaming option

Al,

4.4.2 Decoding Power Init Failures on C3800 Boards

When encountering a power init failure on a board, during diaginit, the busses_on field will indicate that the failure can be located in table B2, when the failure resides between 0x02 and 0x40. This is not entirely true.

An example of a failure in this range is shown below: Notice board number 4 in this example.

```
--> Bay Power Update Returned 00 ppc mask for bpc uart 0
SW Info (DiagIN236): Bay Power Controller status message

PPC Status for BPC number 00
  bay pp   fw   prt bkpln bkpln plt bd bd bd bd bd bd bd bd bay bps bus bus
  cnf cnf   rev   id slot   type typ  0  1  2  3  4  5  6  7  pwr num OK  on
0|ff  ff   ffff ff ff      ff   ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
1|00  00   0205 00 06      02   01 01 00 00 00 00 00 00 00  00  00  00  00
2|00  00   0205 00 07      02   02 02 00 00 00 00 00 00 00  00  01  00  00
3|00  00   0205 00 08      02   06 06 00 00 00 00 00 00 00  00  01  00  00
4|00  00   0205 01 09      03   06 06 00 00 00 00 00 00 00  00  02  f0  37
5|00  00   0205 01 0a      03   02 02 00 00 00 00 00 00 00  00  04  00  00
6|00  00   0205 01 0b      03   01 01 00 00 00 00 00 00 00  00  05  00  00
7|ff  ff   ffff ff ff      ff   ff ff ff ff ff ff ff ff ff  f3  ff  ff  ff
```

Table B2 only displays errors up to 0x28. But the PPC on response codes indicate all failures that can be seen in this range, above 0x22. These errors are detailed in table 4-15.

As can be seen from the example, the busses_on field is a 37, which is past the range in table B2. But, the actual failure can be located in table 4-15. The failure is M4_SETPT_ERR. This indicates that power brick M4 is defective.

For convenience, the entire list in this range is shown below:

0x00	NO_ERROR
0x04	ADC overrange
0x10	PPC +5V out of range
0x11	PPC -5V out of range
0x12	A/D channel 2 out of range
0x13	A/D channel 3 out of range
0x14	A/D channel 4 out of range
0x15	A/D channel 5 out of range
0x16	A/D channel 6 out of range
0x17	A/D channel 7 out of range

.....continued on next page.....

0x22	X2_TRIM_ERR channel 2 trim failed
0x23	X1_TRIM_ERR channel 3 trim failed
0x24	M1_TRIM_ERR channel 4 trim failed
0x25	M2_TRIM_ERR channel 5 trim failed
0x26	M3_TRIM_ERR channel 6 trim failed
0x27	M4_TRIM_ERR channel 7 trim failed
0x28	BUS_NUM_ERR invalid channel id-f/w
0x29	BUS_TYPE_ERR invalid channel type id-f/w
0x32	X2_SETPT_ERR channel 2
0x33	X1_SETPT_ERR channel 3
0x34	M1_SETPT_ERR channel 4
0x35	M2_SETPT_ERR channel 5
0x36	M3_SETPT_ERR channel 6
0x37	M4_SETPT_ERR channel 7
0x3B	NO_XBAR_LOAD no Xbar boards installed
0x40	BRICKS_OFF one or more bricks failed to turn on

Al,

4.4.3 Network Shutdown on C3800 SPU

It is possible for the network on a C3800 work station to shutdown as a result of moving the key-switch from SECURE and then moving it back again. The restarting of the network should be an automatic function, but in this case the file that provides the push to reenable the network has become zeroed and the network remains down. When this takes place it is necessary to "ifconfig" the network back up manually.

The solution to this problem is to edit the spu file:
"/diag/bin/nologin_create".
The file will appear as below:

```
#! /bin/sh

/bin/echo SPU keyswitch is in SECURE position, no logins allowed. >/etc/nologin

# get a list of active networks, don't affect the LOOPBACK
ifconfig -a | grep : | grep UP | grep -v LOOPBACK | grep -v lo0: | sed -e 's/:.*//' > /diag/data/
disabled_networks
```

.....continued on next page.....

```
# now turn off the network connections
if [ -f /diag/data/disabled_networks ]; then
    set `cat /diag/data/disabled_networks`
    while test $# -ge 1
    do
        ifconfig $1 down
        shift
    done
fi
exit 0
```

The entry that begins with ifconfig should be modified as below:

```
if [ ! -f /diag/data/disabled_networks ]; then
    ifconfig -a | grep : | grep UP | grep -v LOOPBACK | grep -v lo0: | sed -e 's/:.*/ /' > /diag/data/
disabled_networks
fi
```

This fix will appear in the next release (after 3.3.1) of the diagnostics.

Al,

4.4.4 ConvexOs on Systems Shipped

All systems that now, and during the past quarter, ship to a customer site have the current shippable ConvexOS loaded on disk 0 of the system. If the drives are shipped separate from a cabinet, the disk containing the OS is marked with a yellow post-it note. If the system drives are shipped in a cabinet, then the drive that contains the OS is located on the lower-left position, as viewed from the front of the cabinet.

Our thanks to Jim Whitmire of Systems Test for this update.

-Kelvyn

4.4.5 Problem with crashdump -H option on C2/C3200 systems

There is an incompatibility with the -H option of crashdump and diagnostic releases 5.0 and 5.1, for the C2.

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The -H switch calls the utility "hwdump" which in turn calls the utility vp_scn in order to dump the vector registers. This utility was found in /mnt/bin and /bin in previous releases. The bottom line is that if this file is missing a full hwdump cannot be performed.

This is not really as bad as it sounds, as in nearly all hwdump's, the vector registers are not required. In addition the diagnostics will leave files alone that it is not necessary to update. This means that many systems that have been updated will still have the vp_scn utility and therefore be unaffected.

The work around for the hwdump is to execute a hwdump_fast instead. This is standard practice anyway, so it should cause few problems.

To correct the crashdump problem, so that a hwdump can be taken, it will be necessary to edit the /mnt/os/crashdump file, on the spu. An example of this portion of crashdump is shown below:

```
# ************************************************************************
#                        Do hardware dump/get comm registers
# ************************************************************************

C1_HWDUMP_DIR="/mnt/jptest"
C2_HWDUMP_DIR="/hw/cputest"
C3_HWDUMP_DIR="/diag/hw"

 if [ "$SPU_ARCH_TYPE" -ge 4 ]          # if neptune, then run diag cleanup
then                                     # this should prevent crashdump
foobar
    if [ -x /diag/bin/dsh ]              # if swip is confused.
    then
        /diag/bin/dsh -c cleanup
        /diag/bin/dsh -c cleanup
    fi
fi
if [ "$DO_HARDWARE_DUMP" -eq 1 ]
then
    if [ "$CPU_TYPE" -eq 1 ]
    then
        cd "$C1_HWDUMP_DIR"
    else
        if [ "$SPU_ARCH_TYPE" -ge 4 ]
        then
            cd "$C3_HWDUMP_DIR"
```

.....continued on next page.....

```
    else
        cd "$C2_HWDUMP_DIR"
    fi
fi

NEW_PWD='pwd'
DUMPFILES="$DUMPFILES $NEW_PWD/$HWDUMP_FILE"
hwdump "$HWDUMP_FILE"
HWDUMP_RESULTS=$?

if [ "$HWDUMP_RESULTS" -ne 0 ]
then
    $ECHO "Hardware dump failed...will not be written to tape"
fi
```

To correct the problem it is necessary to change the following entry:

```
hwdump "$HWDUMP_FILE"
```

to:

```
hwdump_fast "$HWDUMP_FILE"
```

This will enable the vp_scn to be bypassed and allow crashdump to execute the hwdump.

Al,

4.4.6 C2/C3200 Series and PETS 3.0

Because of the numerous wrong answer problems involving C2 series systems and version 3.0 of PETS, as reported in previous tech bulletins, it is recommended that version 2.5 of PETS be run on C2 and C1 series systems.

It will still be necessary to run 3.0 on C3 class systems, but the grief caused on C2's warrants using the previous release of PETS.

A new version of PETS is being qualed, which should solve all of the existing problems with PETS 3.0.

Al,

4.4.7 New C3800 Key Switch Shipping

The greatly anticipated new key switch, for C3800's, is beginning to ship and diagnostic revision 3.3.1 is now available to support it. The switch and software will be shipped automatically. In fact it has already shipped on 7 systems shipped at the end of Q4.

The instructions for installation and a review of its features can be seen in article 32 of Chapter III of the C3800 Troubleshooting Guide. In addition, these instructions will be included with all keys.

Al,

4.4.8 V3.3.1 C3800 Diagnostics

The 3800 diagnostic release 3.3.1 has been released. The following is a list of enhancements and changes for this release.

Please, understand that ppc and bpc firmware is contained in this release, so allowances should be made for time to install. The firmware for each module will take approximately 3 1/2 minutes to download.

SST version 3.1 is a prerequisite for this release. Please ensure that SST is loaded first, or remove the old version before loading 3.3.1 Diagnostics.

POWER SYSTEM CHANGES:

1. Firmware

   BPC firmware is now at revision 3.17 - changes the default bay inlet and outlet temperatures:

   Inlet temps - warm=30 deg C and hot=35 deg C

   Outlet temps - warm=45 deg C and hot=50 deg C

   PPC firmware is now at revision 2.10: fixes primary power (300v) out- of-range problem. Caused message queue to fill up and hang the power system.

2. Utilities

   altsetpts allows user to specify the bay inlet warm/hot temperatures and calculates the outlet warm/hot temperatures (+15 deg C). For example,

.....continued on next page.....

altsetpts -t -w 32 -h 38 bay4
sets the inlet warm temp to 32 deg C and the inlet hot temp to 38 deg C.

diaginit no longer displays the full bay status. Use -v option to get the full report.

/diag/db/set_busses now sets the vtt on the MB board to -2.00V (was -1.95V).

bpcwatchd has been modified to correctly handle "power off" unsolicited messages from the ppc. Now cleans up the Configuration Database to indicate the ppc is powered off.

Software support for the new keyswitch.

UTILITY/TEST ENHANCEMENTS:

1. Utilities

   Added part numbers for RTIOP, new IDC/ITC board and rev C xbar backplane.

   Modified the SPU kernel to fix the window allocation problem (these are main memory windows).

   Added timestamps to cpualloc output for aid in determining down time.

   IA and SP soft errors are now stored in the Configuration Database and can be displayed using dump_soft_log.

   hard_logger now invokes the system_info script when processing APR errors. This includes the same data as when processing a "normal" hard error.

   Added call to the cleanup command in the initall script.

   Added the /etc/shells file to allow users to ftp into the SPU.

2. Diagnostics

   io5000 now supports the RTIOP board.

   Added additional short checking to the sp<->vp and ia8<->xbar tests in subtest 810 of spu4000.

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Added source/sink signal bits to spu4000 subtest 810 error displays.

Added checking so cpu4333 can be run on a single head - cpucti deselects subtests that require 2 or more heads.

modified cu4000 to initialize Xbar in order to clear pre -existing hard errors.

UTILITY/TEST FIXES:

1. Utilities

cpualloc does not clear the cpu_os_req_? flag - allows head to come on- line on next reboot of ConvexOS.

Errintd

No longer attempts to log soft errors from a disabled head

Now disables APR when only a single head exists. APR is re- enabled when another head becomes available.

Now correctly invokes the hard_logger when more than 2 heads pull a hard error.

Fixed initialization of 8247 type SPs in sysreset to enable soft errors - no longer need to edit the /diag/db/scn_ovr file.

Fixed the part number entry for the VIOP board - now accepts all assembly revs.

Fixed ddb so displays tregs in the register display.

Mminit

Fixed intermittent sizing problem - will not need a 2nd run.

Disallows downsizing of 256MB size boards to 128MB.

2. Tests

Fixed timeout problems in cpucti when running cpu4331 in chain mode.

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The SPU version of idcfmt now works, i.e. can format a disk.

Other fixes:

cpualloc.test now returns a 0 if no SST data patterns exists. Head will come on-line even if SST is never run.

The correct version of scan_trace is now installed - this is the 1X version.

Updated version of nts.

Can now specify parameters to mtst on command line:

mtst -d <addr> <byte_cnt> <xfr_type> <opcode> <even_pat> <odd_pat>

adb is now part of the diagnostic release.

CXTS SUPPORT:

All error logging now uses RPC instead of system V IPC.

xsfp has a new boot option: cxts control boot.

xsfp starts 3 new daemons:

cxts_rt.prt

cxts_server.prt

cxts_ui

If CXTS daemons are not found, i.e. CXTS is not loaded, an error is printed in SPU Console window.

If CXTS daemons are found then startup of X environment after a SPU boot will take longer.

The "RPC: Program not registered" message during SPU boot can be ignored.

Any compiled user programs that log events need to be recompiled.

Al,

4.4.9 C3400 8 Head JSM Error Codes

8 Head JSM Error and Message Codes
firmware revision 1.2

Code	Error/ Message
00	Deadman timer indicates JSM internal problem
02	SP-SM.PWRINTAK* failure
04	SP-SM.SMBDATA<7..0>* failure
07	SP-SM.SPUDCOK failure
08	A/D Convertor Timed Out
0B	SP4 Illegal Instruction
0D	SP4 instruction cycle timed out
14	CPU7 installed incorrectly
15	CPU3 installed incorrectly
1A	CPU6 installed incorrectly
1B	CPU2 installed incorrectly
1C	SP4 installed incorrectly
1D	CUJ installed incorrectly
1E	ME0 installed incorrectly
1F	MO0 installed incorrectly
20	ME1 installed incorrectly
21	MO1 installed incorrectly
22	ME2 installed incorrectly
23	MO2 installed incorrectly
24	ME3 installed incorrectly
25	MO3 installed incorrectly
27	CPU1 installed incorrectly
28	CPU5 installed incorrectly
2D	CPU0 installed incorrectly
2E	CPU4 installed incorrectly
33	PIX installed incorrectly
34	PIY installed incorrectly
41	PS1 power supply temp failure
42	PS2 power supply temp failure
43	PS3 power supply temp failure

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44	PS4 power supply temp failure
45	PS5 power supply temp failure
46	PS6 power supply temp failure
47	PS7 power supply temp failure
48	PS8 power supply temp failure
49	PS9 power supply temp failure
4A	PS10 power supply temp failure
4B	PS11 power supply temp failure
_	
61	AC power failure, check JSM board
62	AC power failure, check JSM board
_	
71	+5.0V DC power supply failure
72	+12.0V DC power supply failure
73	-12.0V DC power supply failure
74	-5.0V DC power supply failure
75	-4.5V DC power supply failure
76	-2.0V DC power supply failure
77	-5.2V DC power supply failure
_	
81	PS1 current sharing failure
82	PS2 current sharing failure
83	PS3 current sharing failure
84	PS4 current sharing failure
85	PS5 current sharing failure
86	PS6 current sharing failure
87	PS7 current sharing failure
88	PS8 current sharing failure
89	PS9 current sharing failure
8A	PS10 current sharing failure
8B	PS11 current sharing failure
_	
91	-4.5V current sharing out of tolerance
92	-2V current sharing out of tolerance
93	+5V current sharing out of tolerance
_	
A0	Front card cage intake thermistor exceeds tolerance
A1	Rear card cage exhaust thermistor exceeds tolerance
A2	PI2 terminator thermistor exceeds tolerance

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A3	JSM thermistor exceeds tolerance
A4	Front card cage exhaust thermistor exceeds tolerance
A5	Power supply exhaust thermistor exceeds tolerance
B1	CUJ airflow failure
B2	PIY airflow failure
C0	Insufficient power supplies for configuration
E1	FN1 failure
E2	FN2 failure
E3	FN3 failure
E4	FN4 failure
E5	FN5 failure
E6	FN6 failure
E7	FN7 failure
E8	FN8 failure

Dan Brenner